

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHM, MLB, M96  
EVT  
08/01/2008

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE



Page	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram	WFERRY-WF	05/11/2006
3	Power Block Diagram	POWER	06/30/2005
4	CONFIGURATION OPTIONS	(N/A)	(N/A)
5	Acoustic Cap BOM Config Tables	N/A	N/A
6	Functional Test and No-Tests	(MASTER)	(MASTER)
7	Power Aliases	WFERRY	06/15/2006
8	SIGNAL ALIAS /RESET	(MASTER)	(MASTER)
9	CPU FSB	M97	02/04/2008
10	CPU Power & Ground	(MASTER)	(MASTER)
11	CPU Decoupling & VID	MSARWAR	04/26/2006
12	eXtended Debug Port (XDP)	M97	02/04/2008
13	MCP CPU Interface	M97	02/04/2008
14	MCP Memory Interface	M97	02/04/2008
15	MCP Memory Misc	M97	02/04/2008
16	MCP PCIe Interfaces	M97	02/04/2008
17	MCP Ethernet & Graphics	M97	02/04/2008
18	MCP PCI & LPC	M97	02/04/2008
19	MCP SATA & USB	M97	02/04/2008
20	MCP HDA & MISC	M97	02/04/2008
21	MCP Power & Ground	M97	02/04/2008
22	MCP Standard Decoupling	M97	02/04/2008
23	MCP Graphics Support	M97	02/04/2008
24	SB Misc	M97	02/04/2008
25	FSB/DDR3 Vref Margining	BEN	01/15/2008
26	DDR3 Support	T18_MLB	01/30/2008
27	DDR3 DRAM Channel A (0-31)	(MASTER)	(MASTER)
28	DDR3 DRAM Channel A (32-63)		
29	DDR3 DRAM Channel B (0-31)	(MASTER)	(MASTER)
30	DDR3 DRAM Channel B (32-63)		
31	DDR BYPASSING 1	MEMORY	06/20/2005
32	DDR BYPASSING 2	MEMORY	06/20/2005
33	Memory Active Termination	M70	01/09/2007
34	Wireless M93 Connector	M70	01/09/2007
35	Hatch and Audio Connectors	(MASTER)	(MASTER)
36	SATA Connectors	CHANGZHANG	02/05/2008
37	USB EXTERNAL CONNECTORS	M70	01/09/2007
38	IPD Connector		
39	SMC	M97	02/21/2008
40	SMC SUPPORT	M70	01/09/2007
41	LPC+SPI Debug Connector	CHANGZHANG	01/24/2008

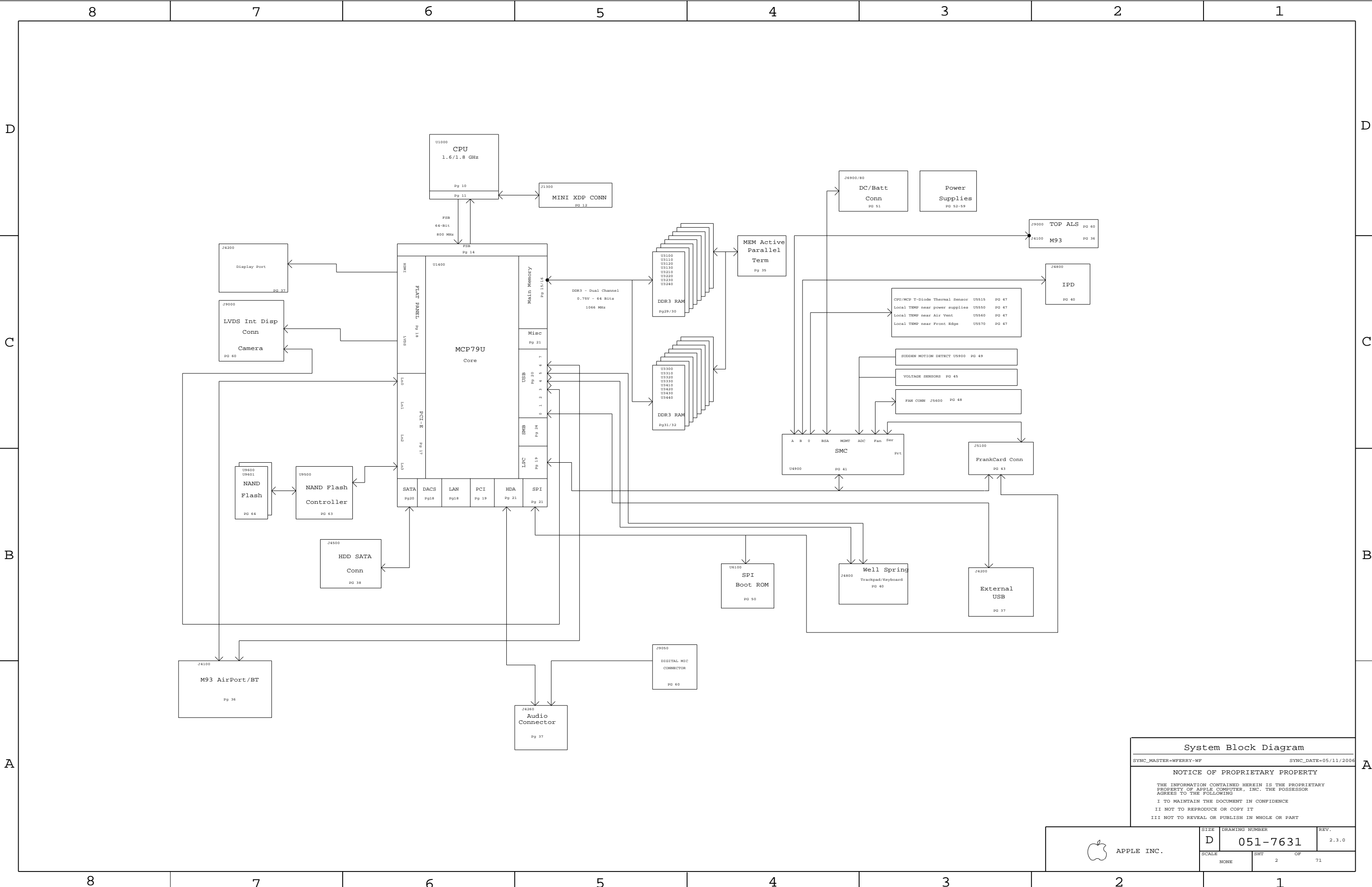
Page		Contents	Sync		Date
42	52	M97 SMBUS CONNECTIONS	BEN		02/04/2008
43	53	Voltage Sensors	M70		01/09/2007
44	54	Current Sensing	YUNWU		02/04/2008
45	55	TEMPERATURE SENSORS	M70		01/09/2007
46	56	Fan	M70		01/09/2007
47	59	Sudden Motion Sensor (SMS)	M76_MLB		01/12/2007
48	61	SPI ROM	CHANGZHANG		02/15/2008
49	69	DC-In & Battery Connectors	M70		01/09/2007
50	71	IMVP6 CPU VCore Regulator	POWER		07/13/2005
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52	73	1.8V LDO Supply			
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54	75	1.5V/0.75V Supplies	M70		01/09/2007
55	76	5V / 3.3V Power Supply	RXU_K20		05/21/2008
56	77	POWER SEQUENCING	YUAN_MA		02/04/2008
57	78	POWER FETS	YUAN_MA		02/04/2008
58	79	PBUS Supply/Battery Charger	M70		01/09/2007
59	90	LVDS,Camera Conn. and ALS Conn.	GPU		06/23/2006
60	93	DISPLAYPORT SUPPORT	NMARTIN		12/18/2007
61	94	DisplayPort Connector	M98_MLB		01/17/2008
62	97	LED Backlight Driver	(MASTER)	(MASTER)	
63	98	LCD Backlight Support	M97		02/04/2008
64	99	Additional CPU/GPU Decoupling			
65	100	CPU/FSB Constraints	M97		02/04/2008
66	101	Memory Constraints	M97		02/04/2008
67	102	MCP Constraints 1	M97		02/04/2008
68	103	MCP Constraints 2	M97		02/04/2008
69	106	SMC Constraints	M97		02/04/2008
70	108	M96 Power and Ground Nets	(MASTER)	(MASTER)	
71	109	M96 RULE DEFINITIONS	M97		02/04/2008

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7631	1	SCHEM, MLB, M96	SCH	CRITICAL	
820-2375	1	PCBF, MLB, M96	PCB	CRITICAL	

DRAWING  
TITLE=M96\_MLB  
ABBREV=DRAWING  
LAST\_MODIFIED=Fri Aug 1 09:54:13 2008

<div>DIMENSIONS ARE IN MILLIMETERS</div> <div>XX ± _____</div> <div>X.XX ± _____</div> <div>X.XXX ± _____</div> <div>ANGLES ± _____</div> <div>DO NOT SCALE DRAWING</div>	METRIC			<div> APPLE INC.</div>	
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	DRAFTER	<div><div></div><div></div></div>	DESIGN CK	<div><div></div><div></div></div>	TITLE
	ENG APPD	<div><div></div><div></div></div>	MFG APPD	<div><div></div><div></div></div>	
QA APPD	<div><div></div><div></div></div>	DESIGNER	<div><div></div><div></div></div>		
<div></div> <div>THIRD ANGLE PROJECTION</div>	RELEASE	<div><div></div><div></div></div>	SCALE NONE		SCHEM, MLB, M96
	MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D		
			DRAWING NUMBER 051-7631		REV. 2.3.0
		SHT 1 OF 71			



System Block Diagram

SYNC\_MASTER=WFERRY-WF

SYNC\_DATE=05/11/2006

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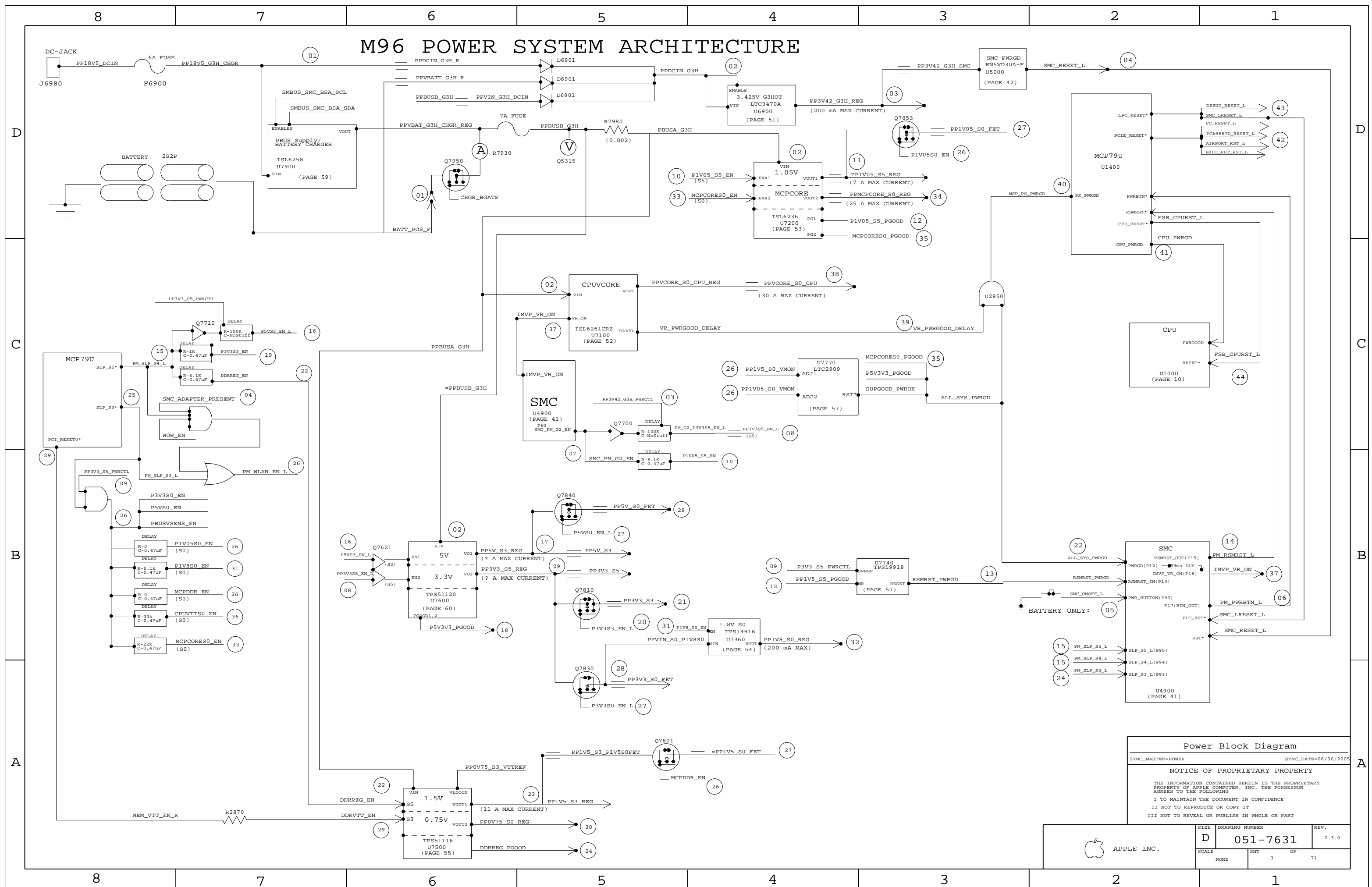
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SCALE		SHT	OF	
NONE		2	71	

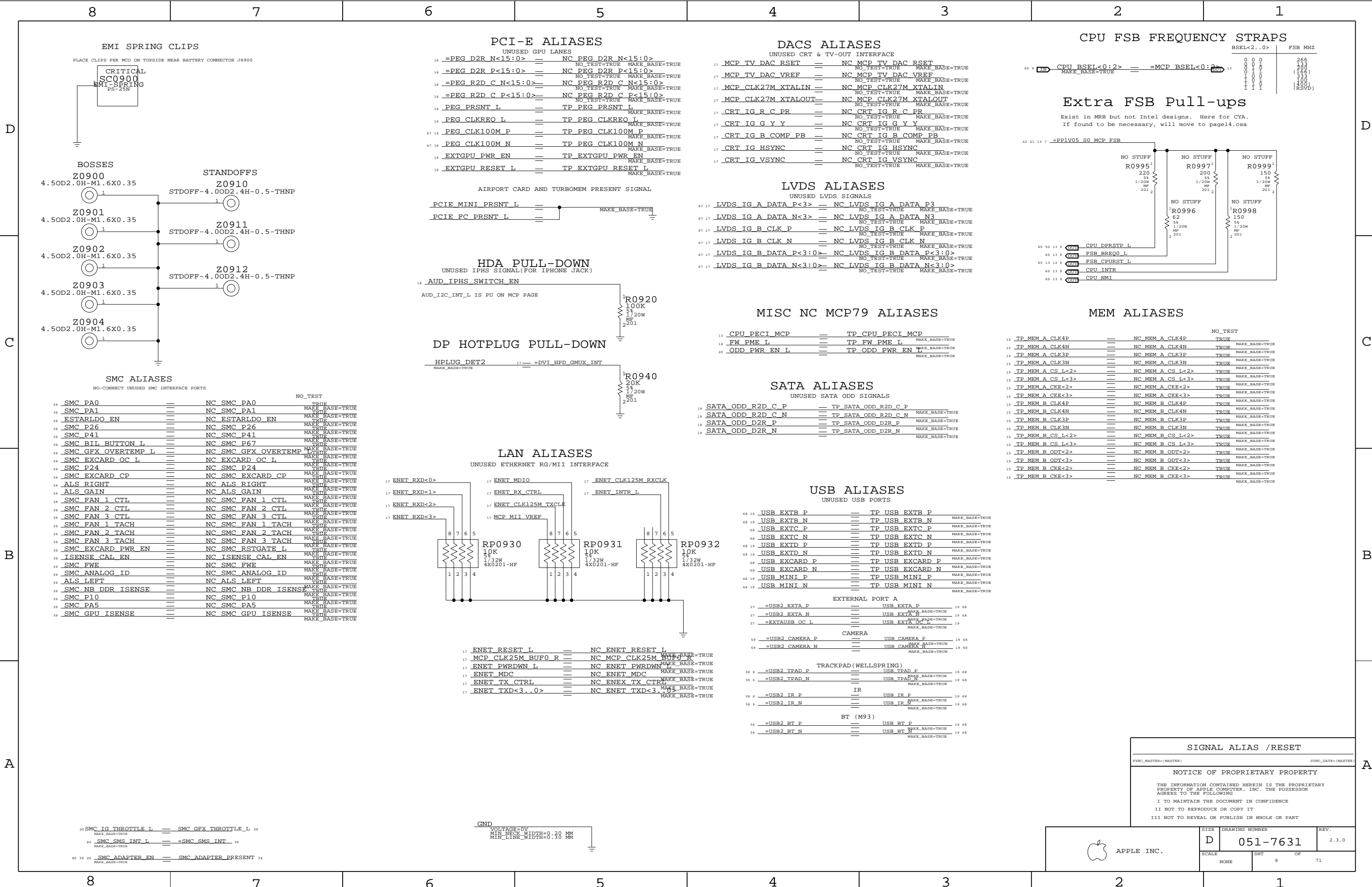




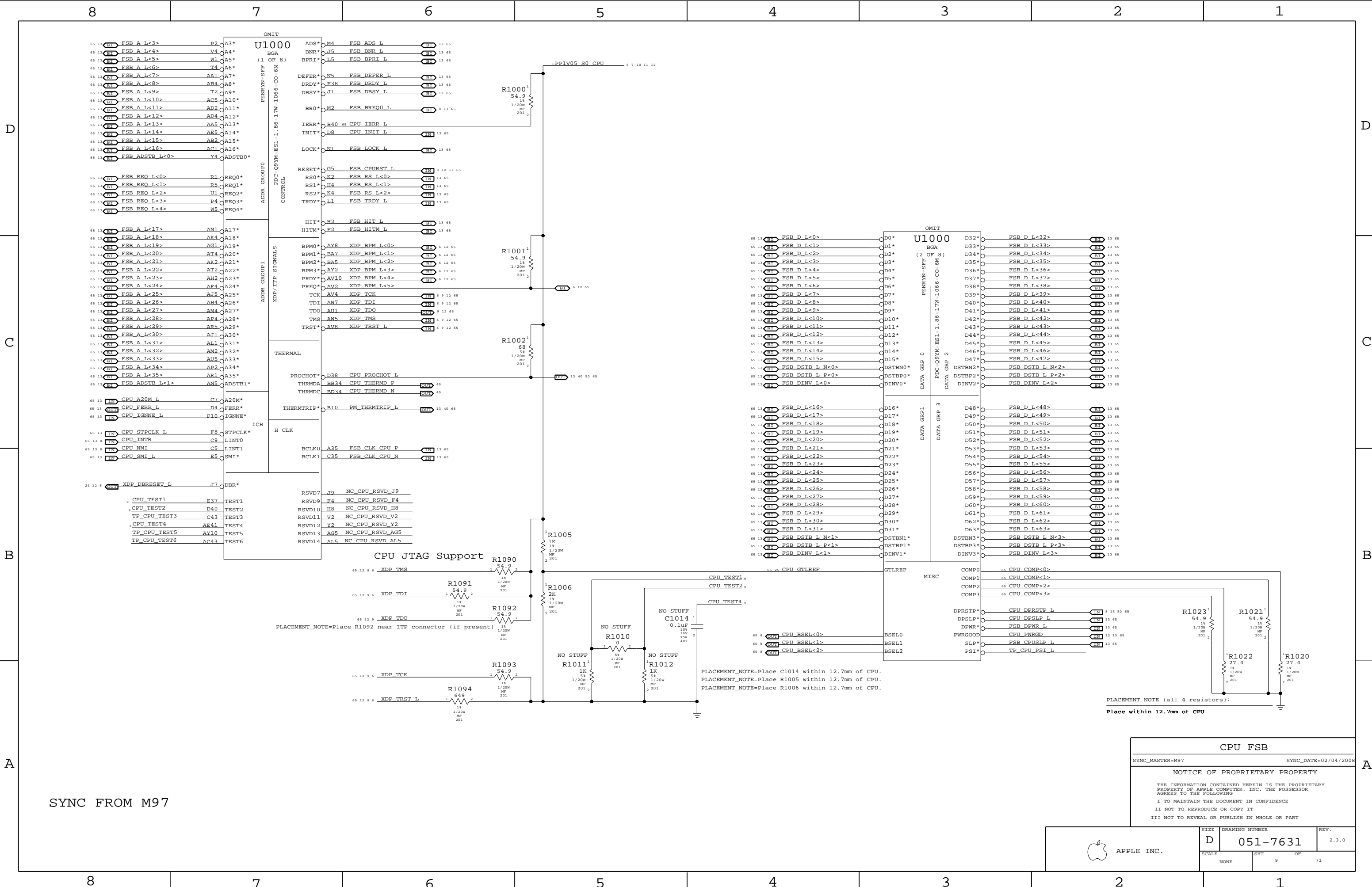












SYNC FROM M97

CPU FSB

SYNC\_MASTER=M97

SYNC\_DATE=02/04/2008

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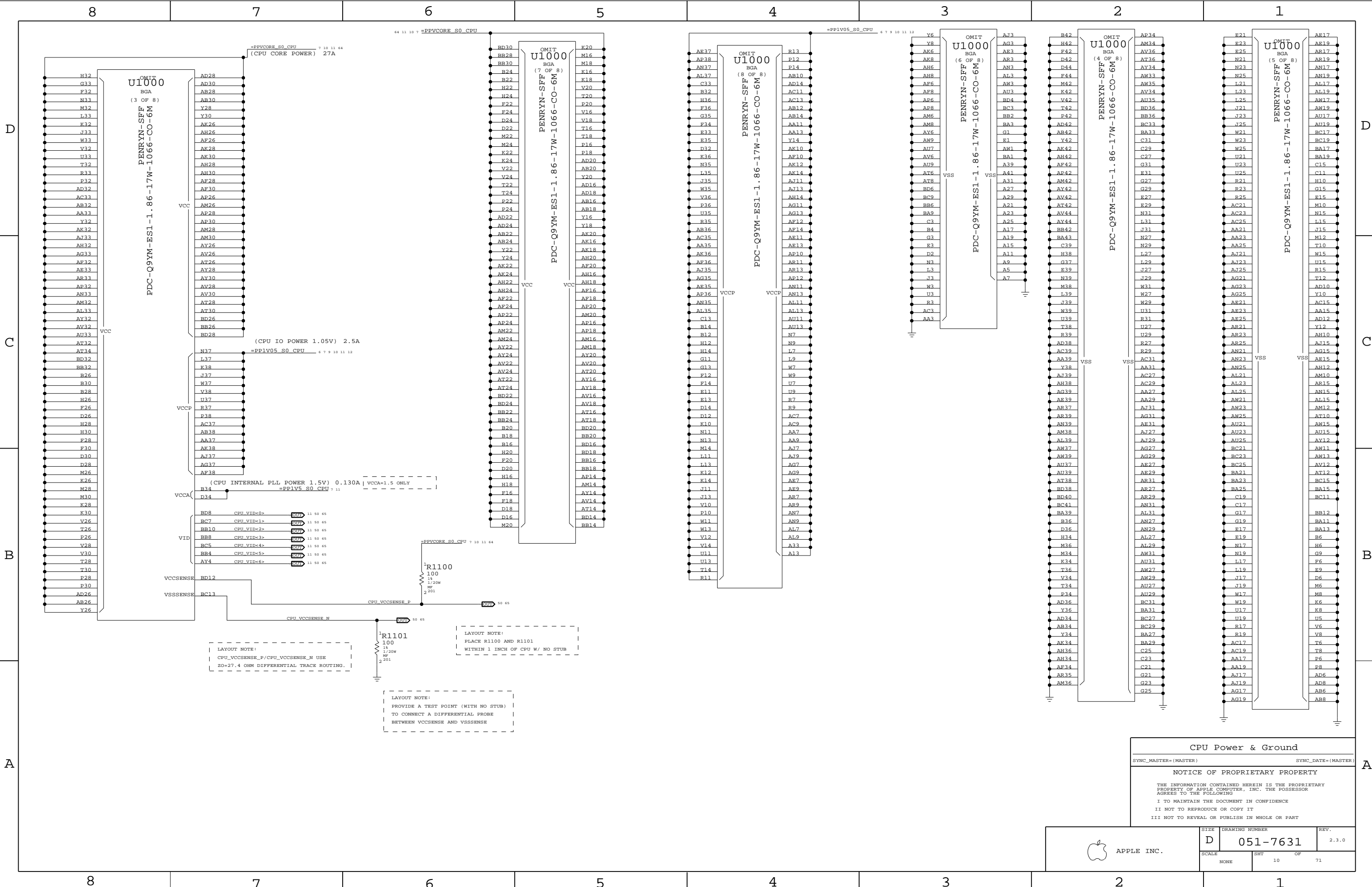
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CPU Power & Ground

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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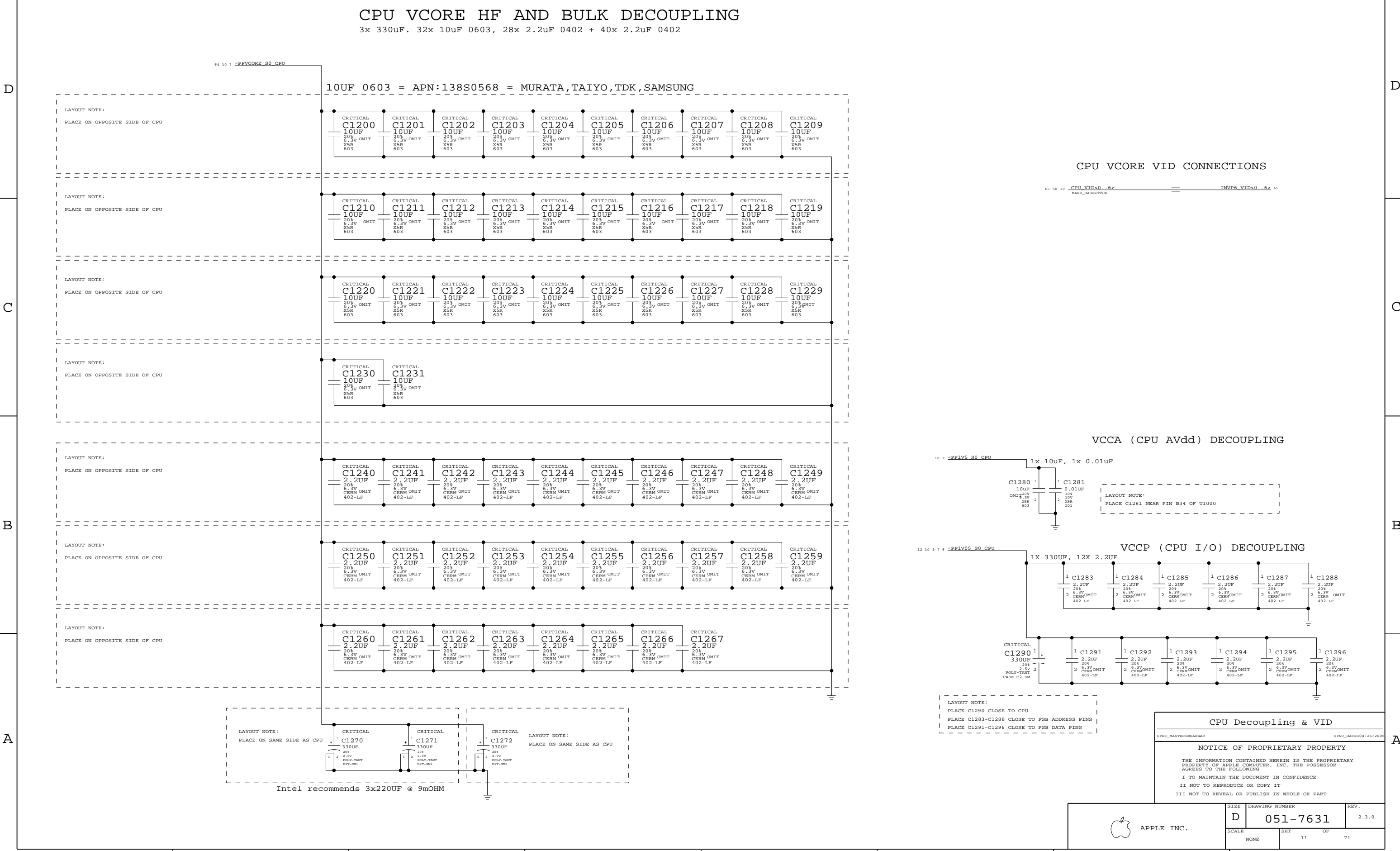
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SCALE		SHT	OF
NONE		10	71


8	7	6	5	4	3	2	1
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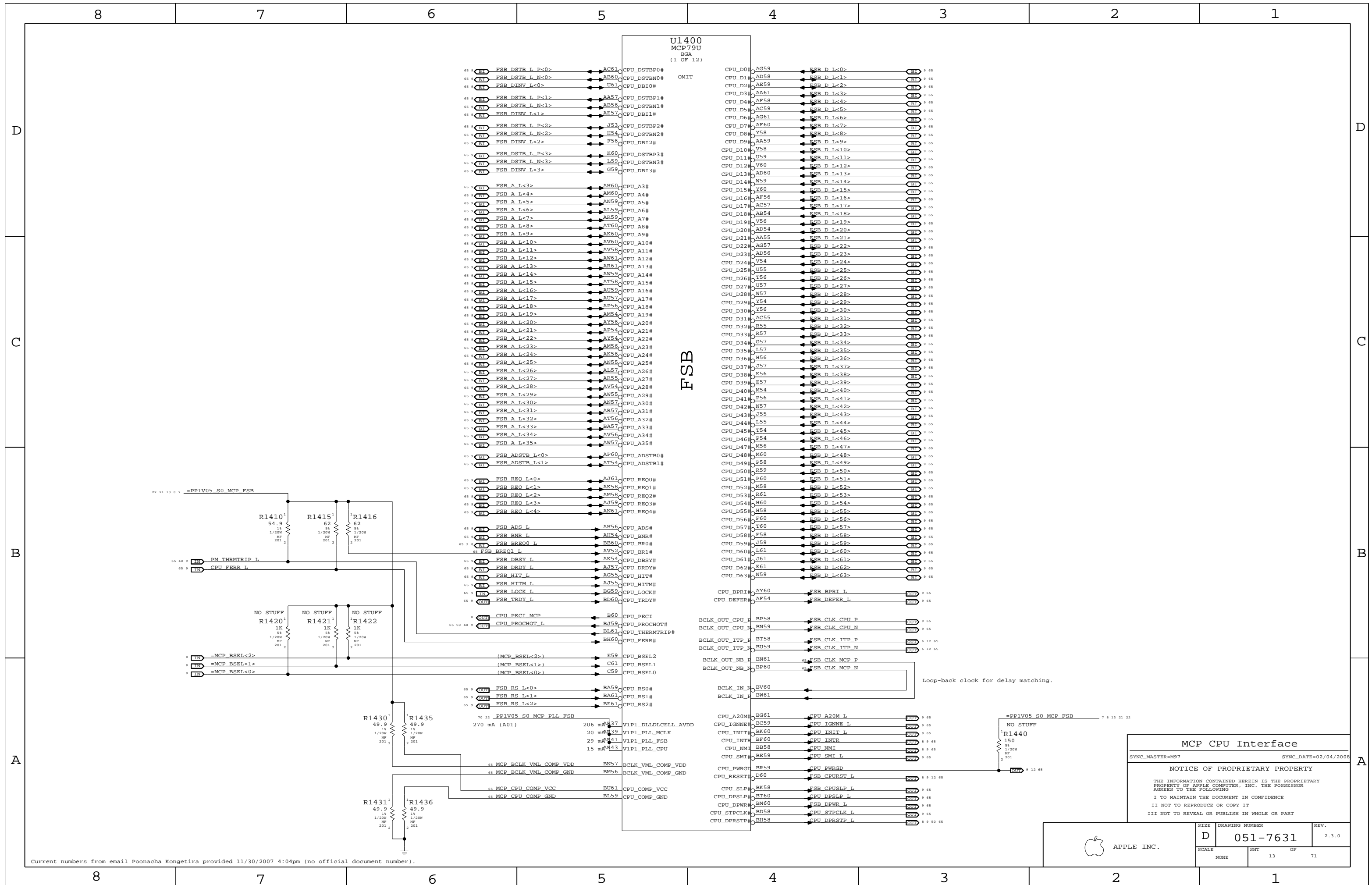
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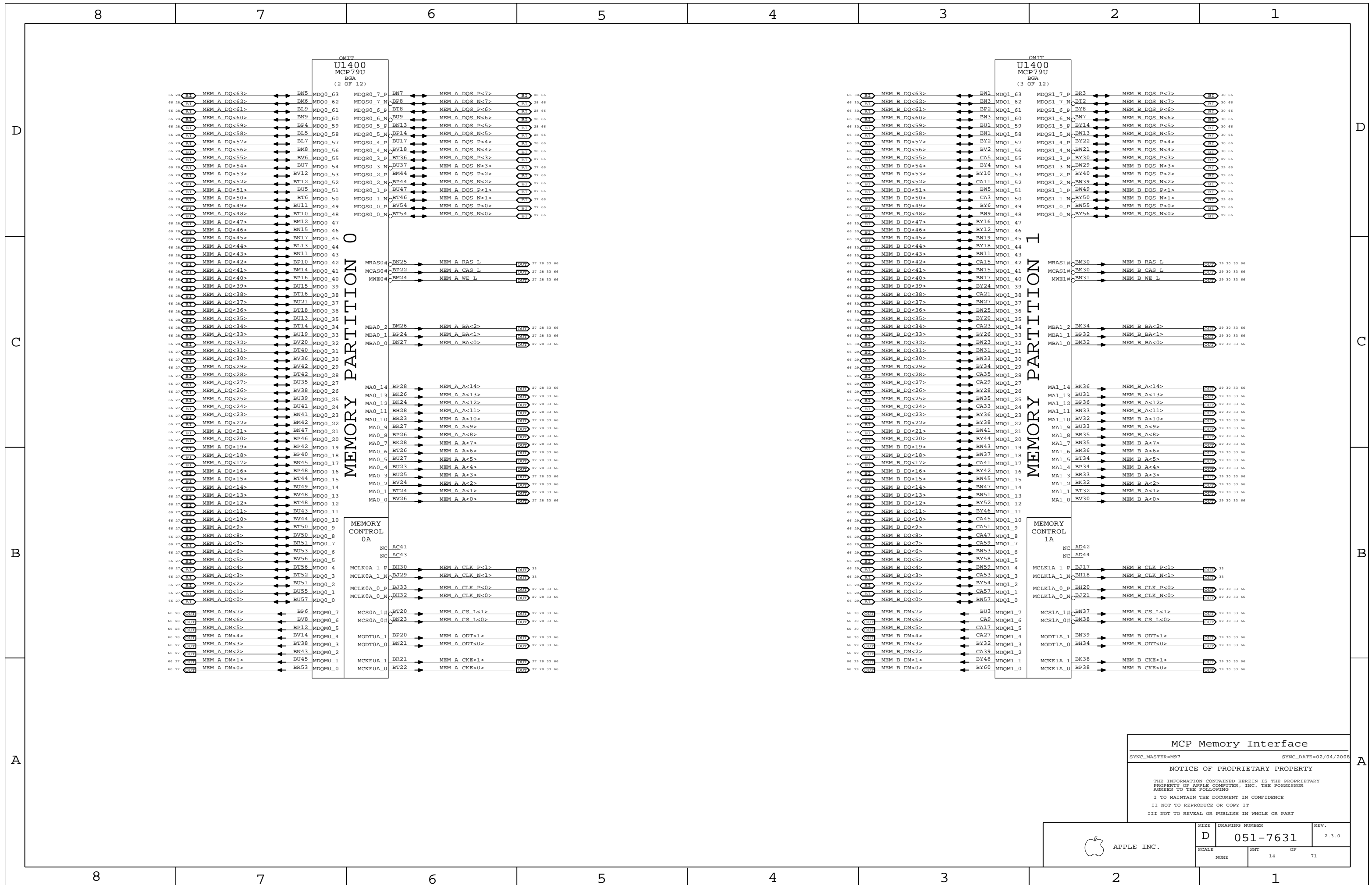
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 APPLE INC.

SIZE	DRAWING NUMBER
D	051-







D

C

B

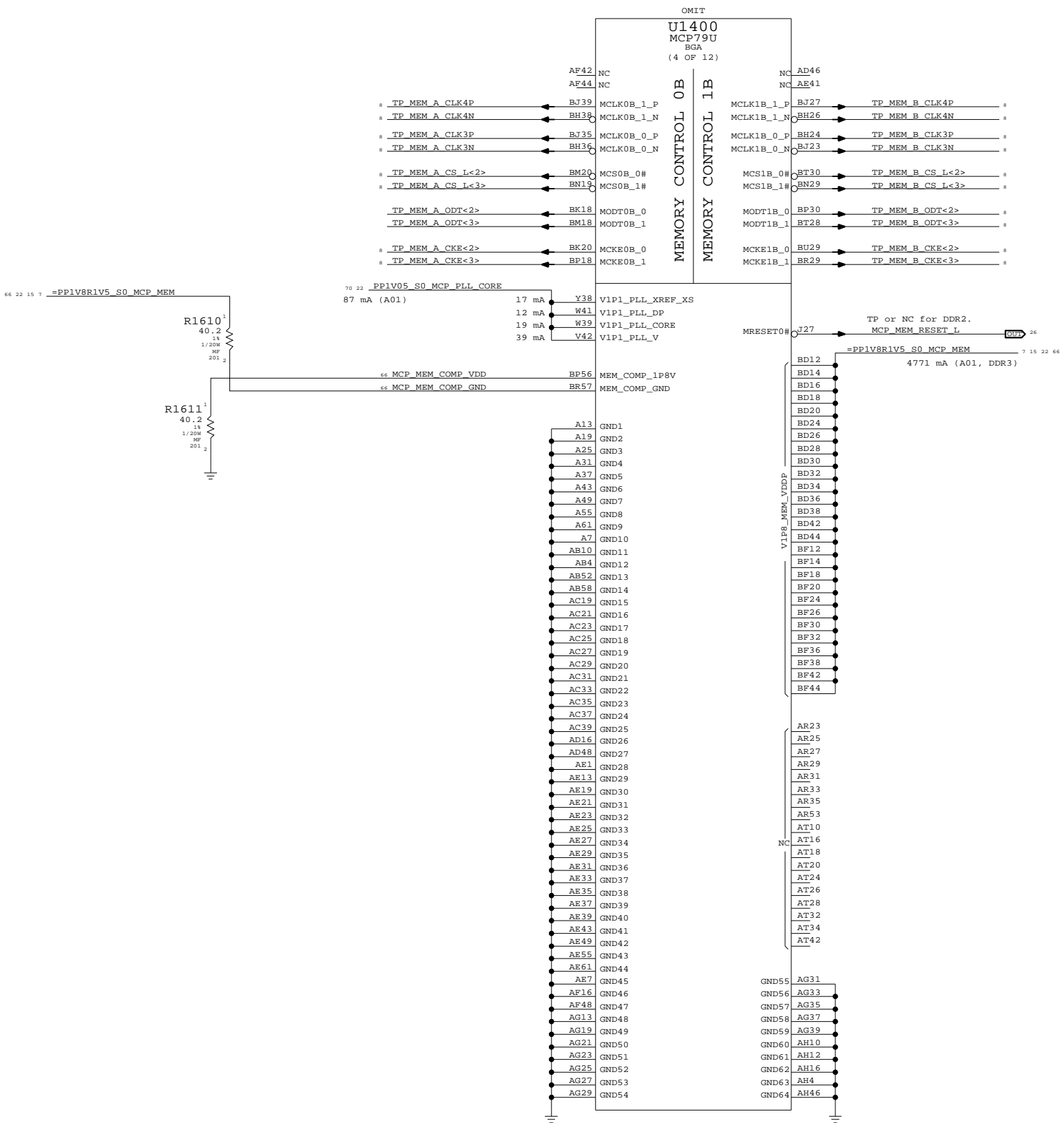
A

D

C

B

A



MCP Memory Misc

SYNC\_MASTER=M97

SYNC\_DATE=02/04/2008


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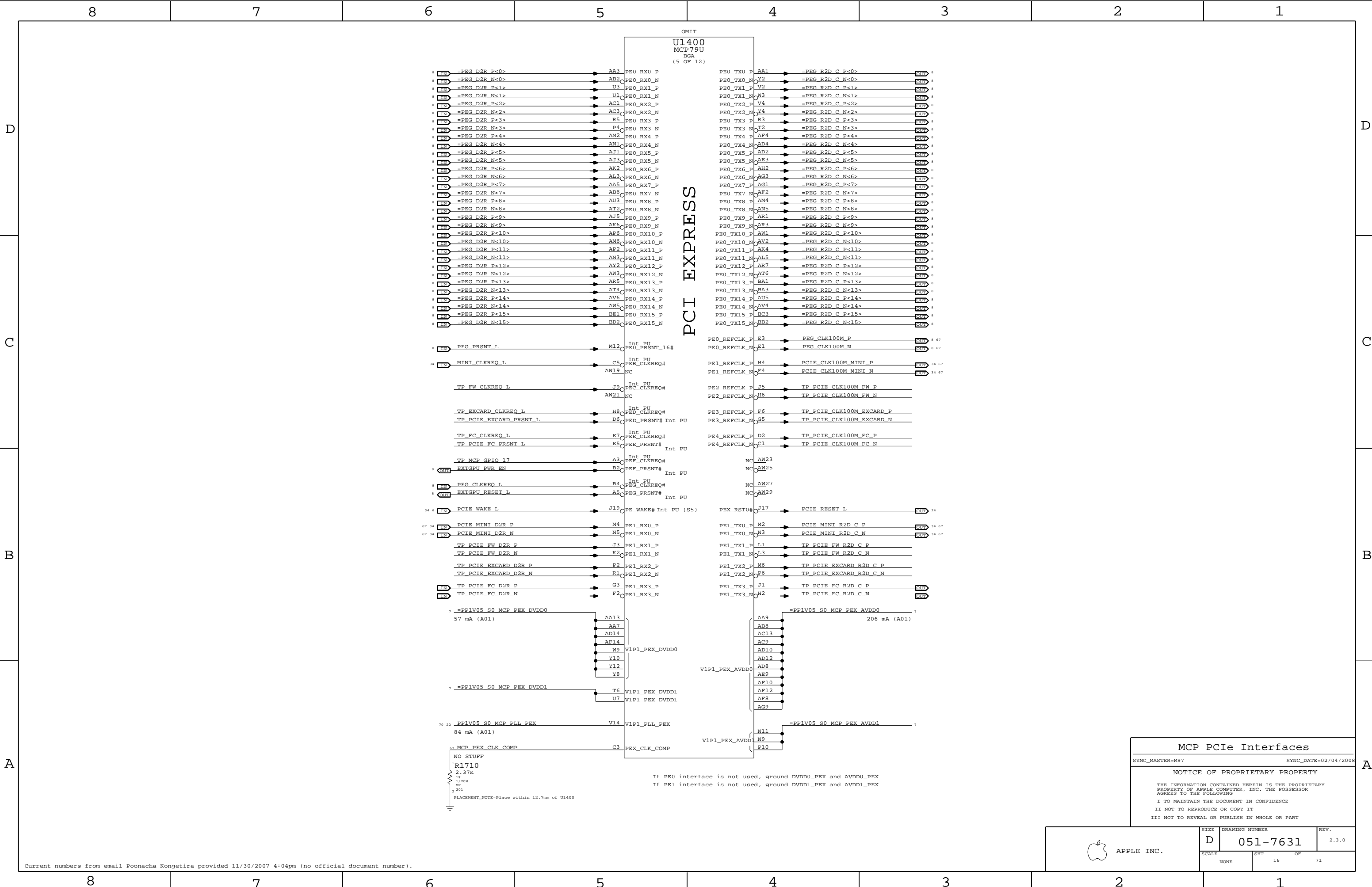
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SCALE		SHT	OF	REV.
NONE		15	71	



MCP PCIe Interfaces

SYNC\_MASTER=M97

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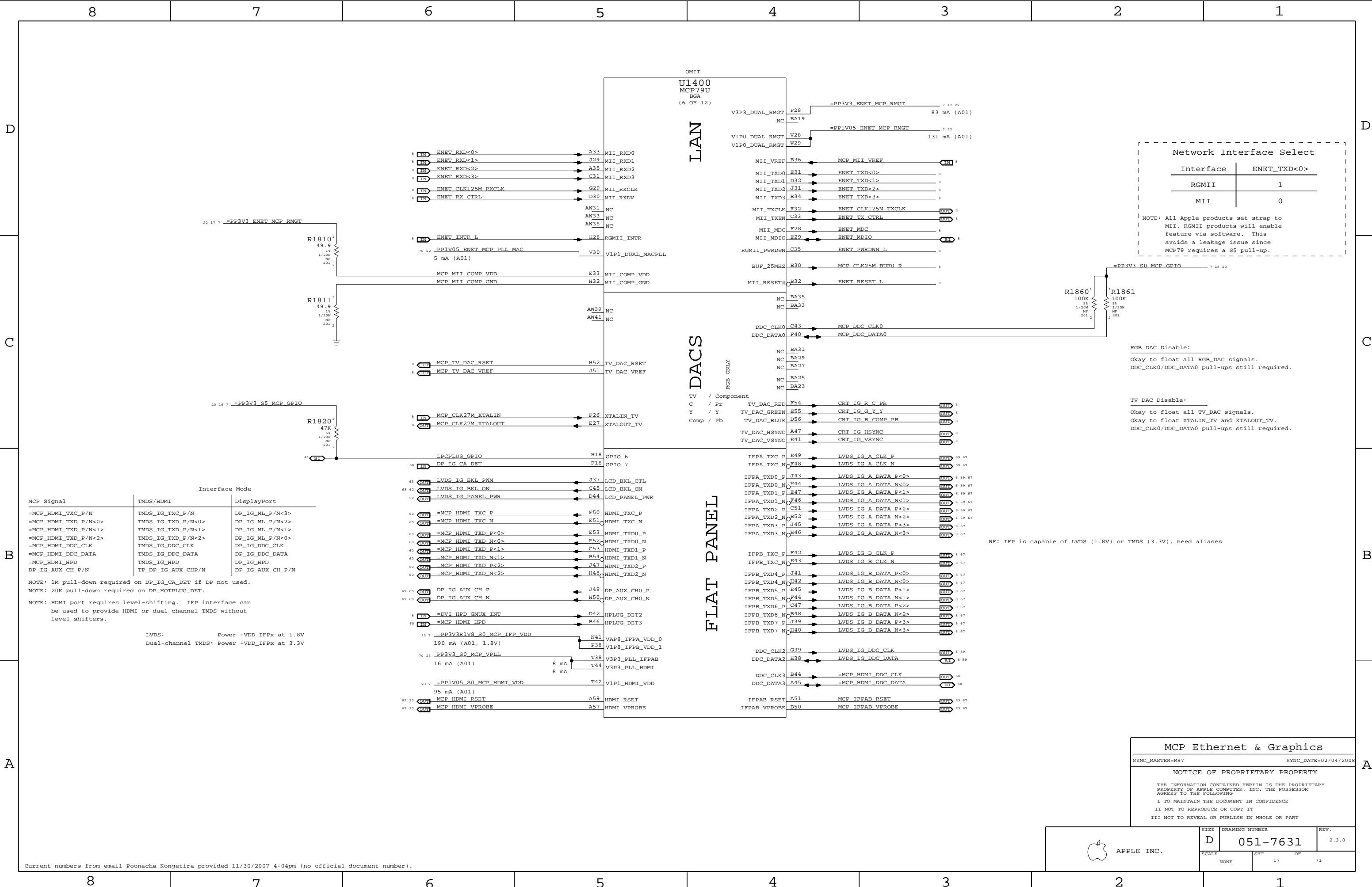
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SCALE		SHT	OF	REV.
NONE		16	71	





MCP Ethernet & Graphics

SYNC\_MASTER=M97

SYNC\_DATE=02/04/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7631

REV.

2.3.0

SCALE

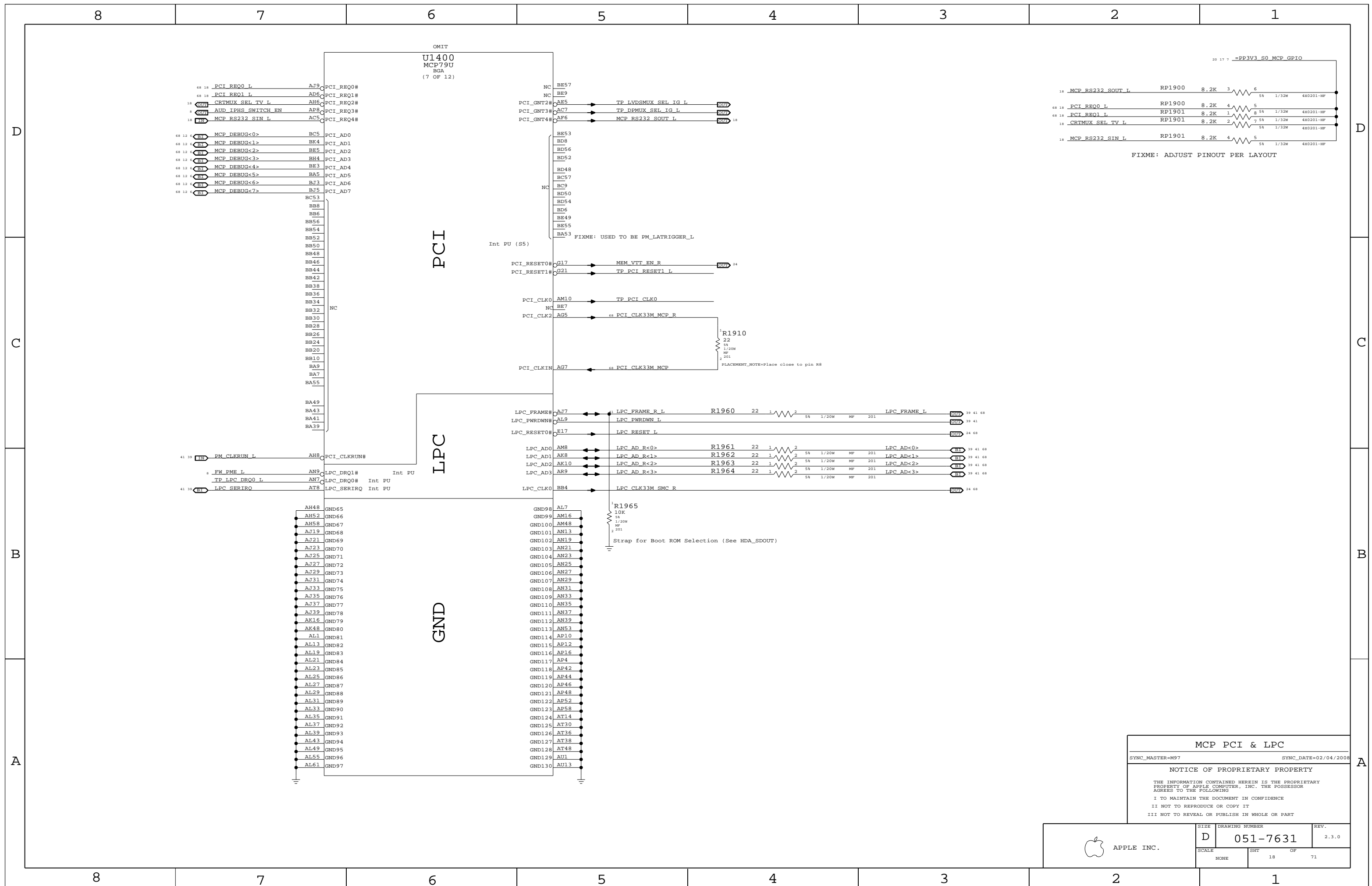
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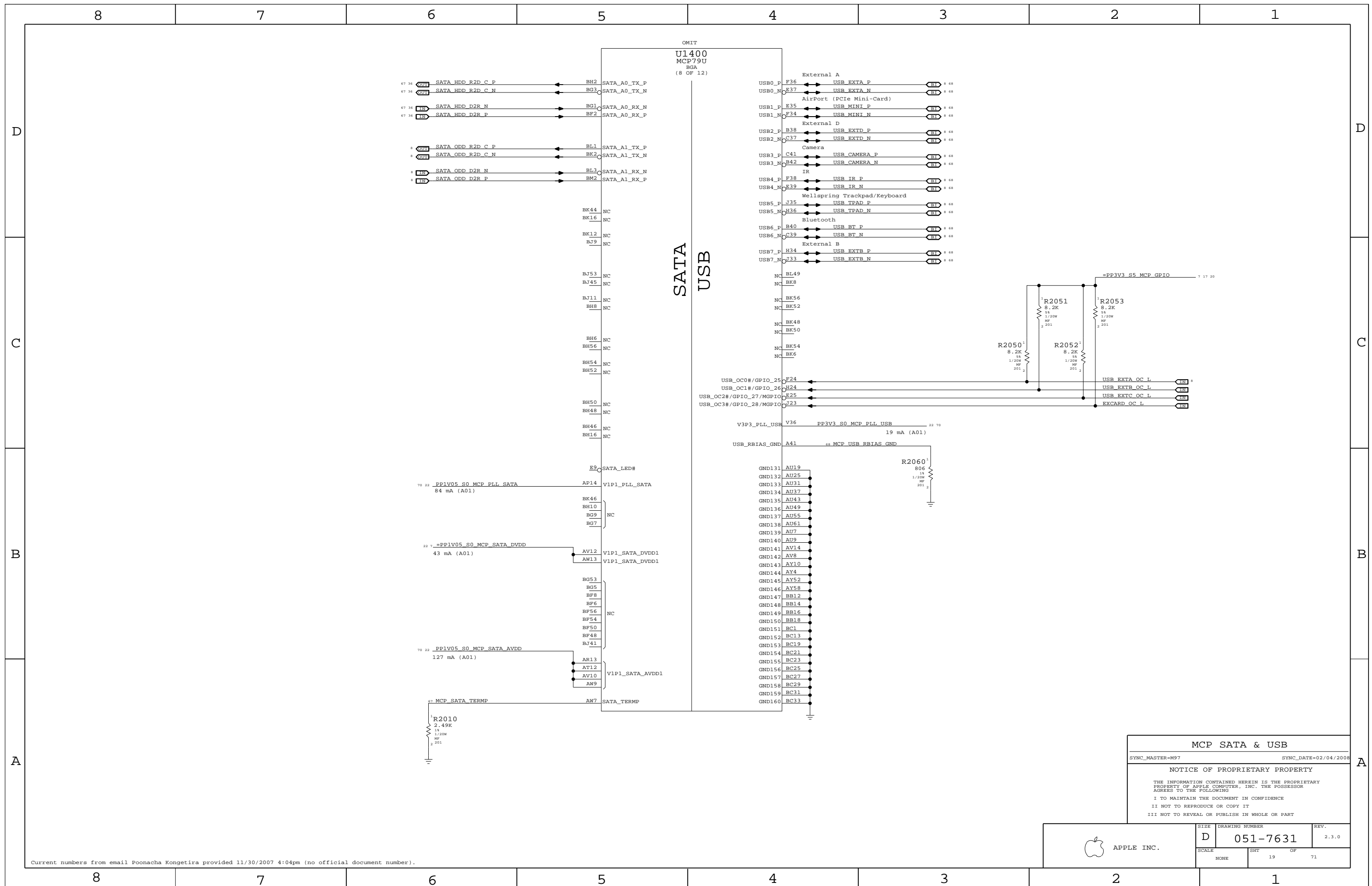
SHT

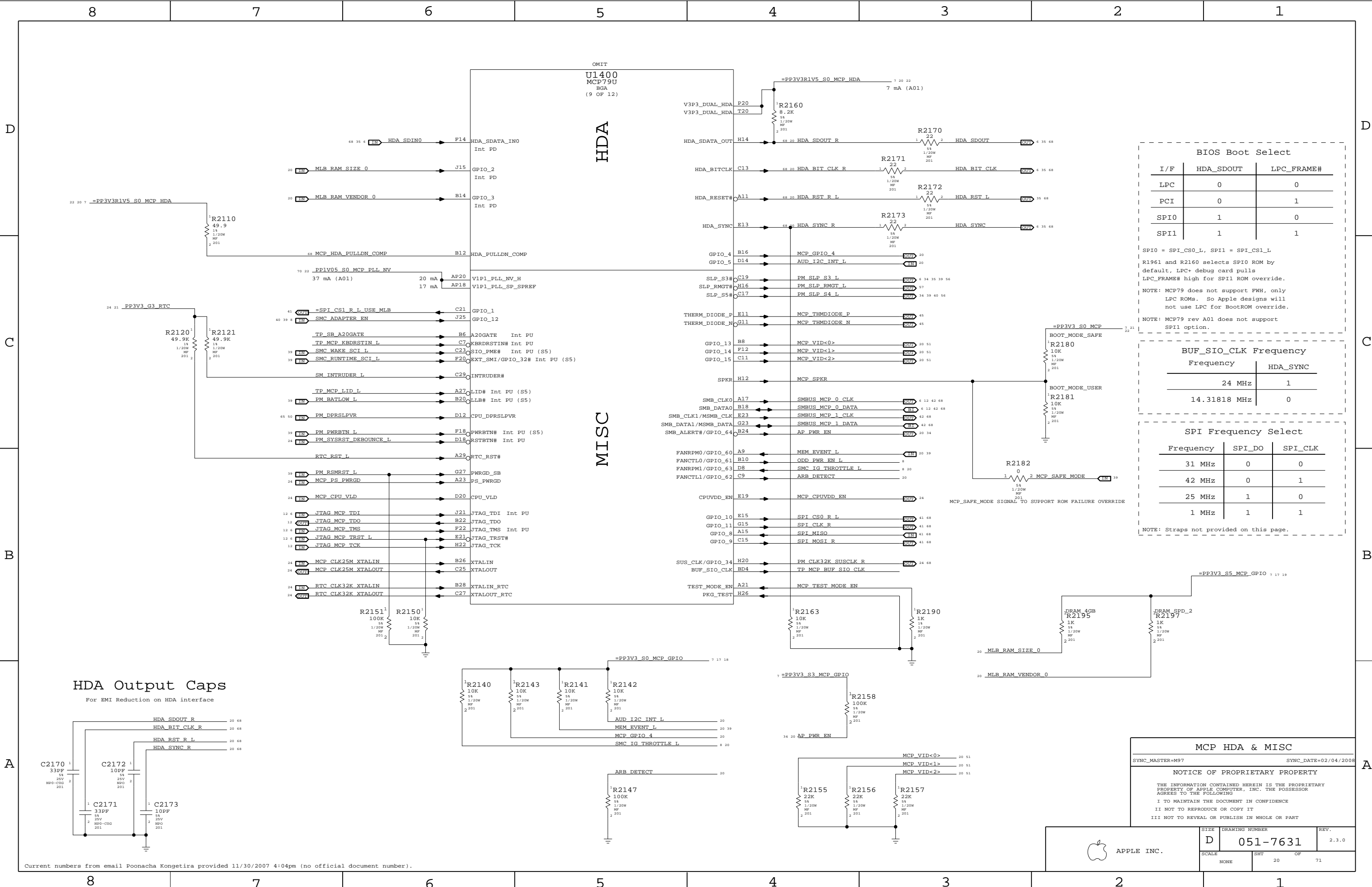
17

OF

71







BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI\_CS0\_L, SPI1 = SPI\_CS1\_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC\_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option.

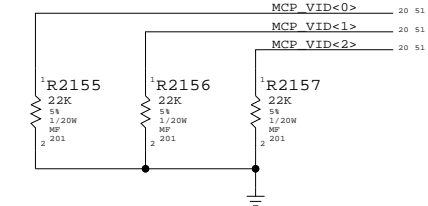
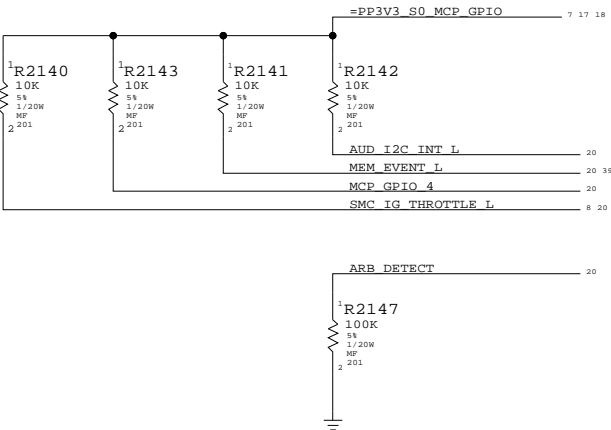
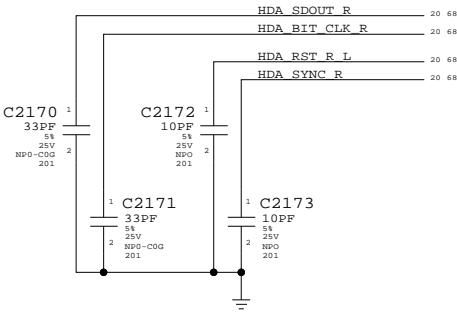
BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

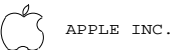
NOTE: Straps not provided on this page.

### HDA Output Caps

For EMI Reduction on HDA interface

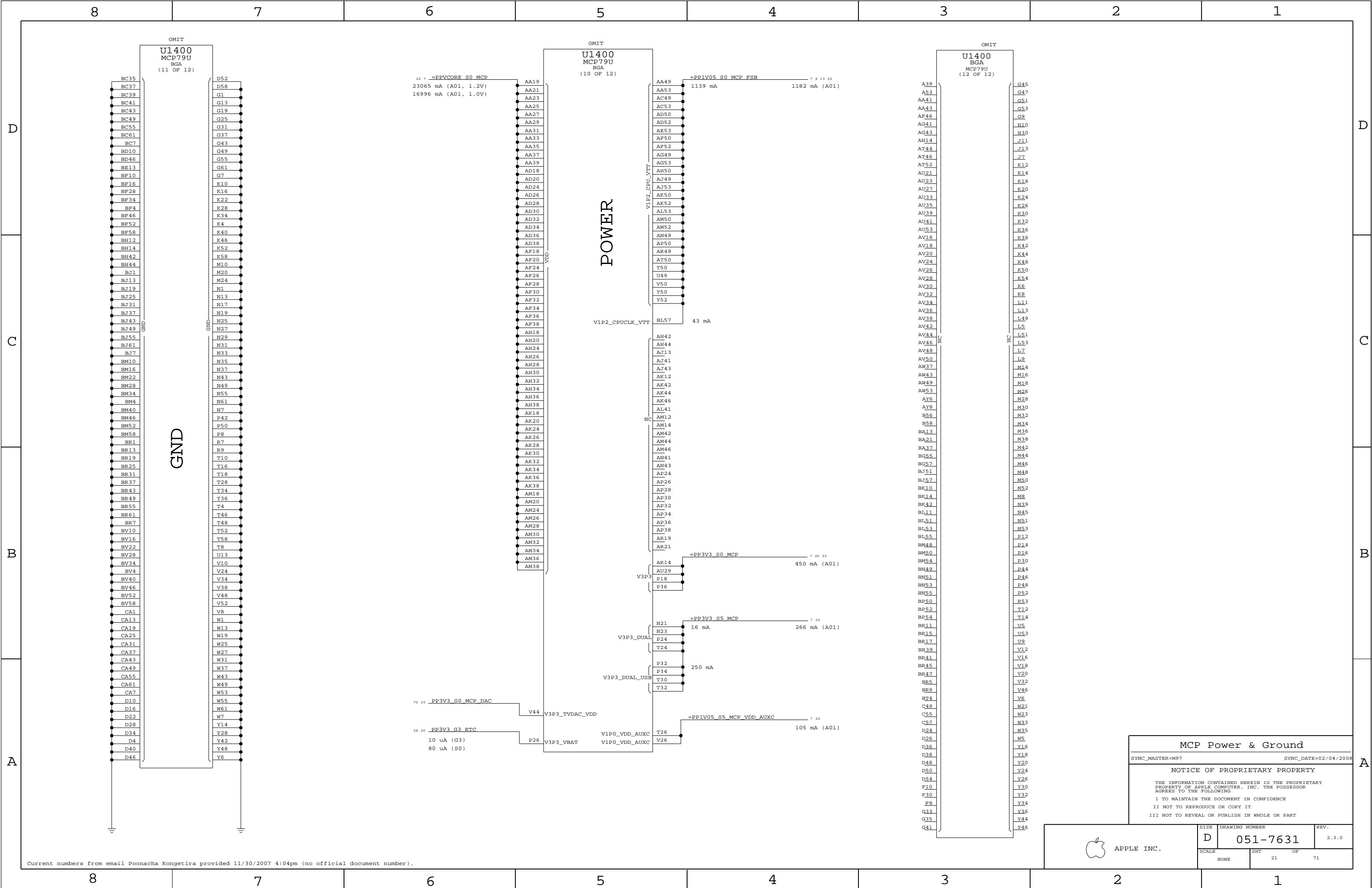


MCP HDA & MISC		
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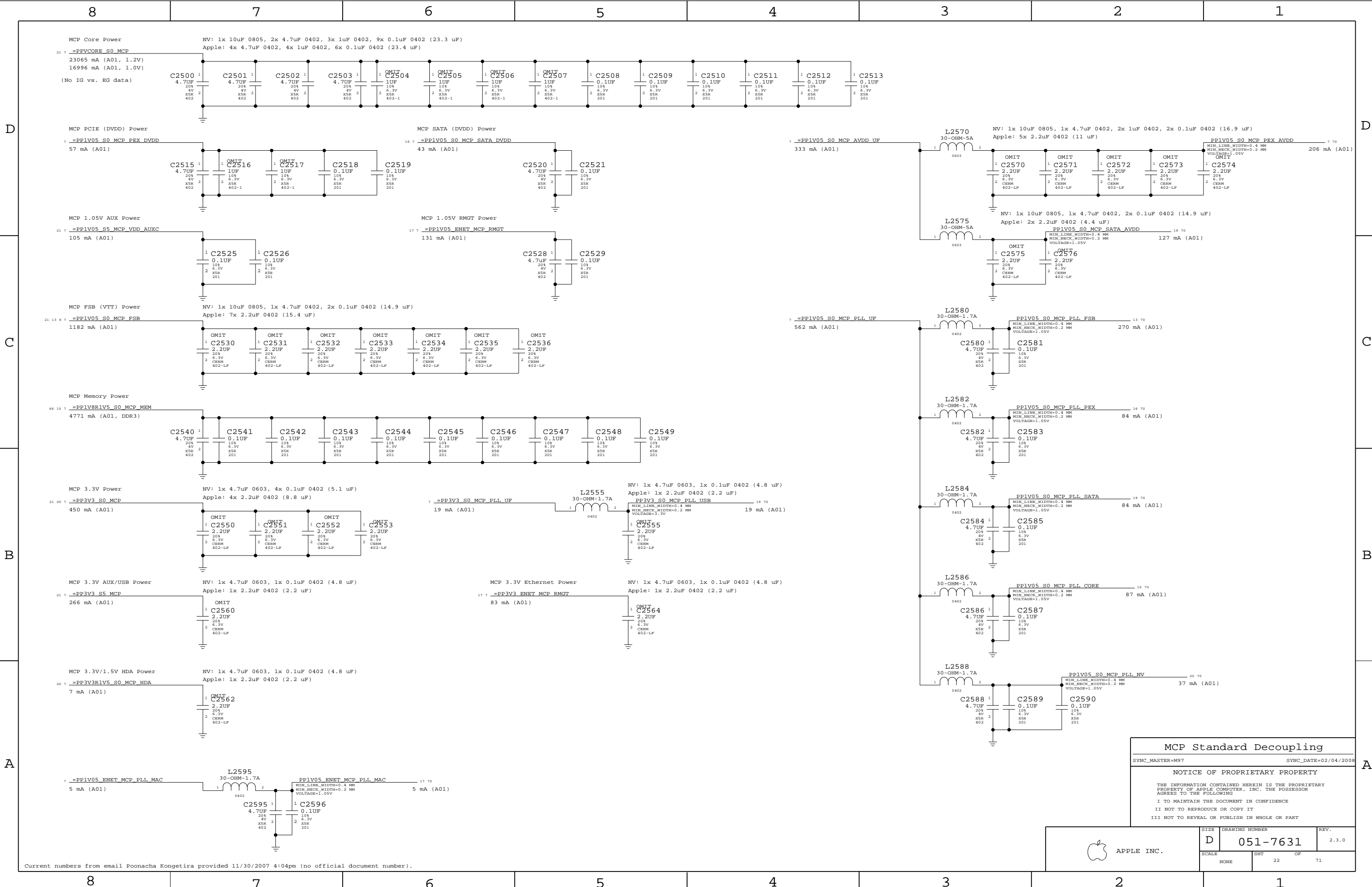


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NONE	20	71



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MCP Standard Decoupling

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

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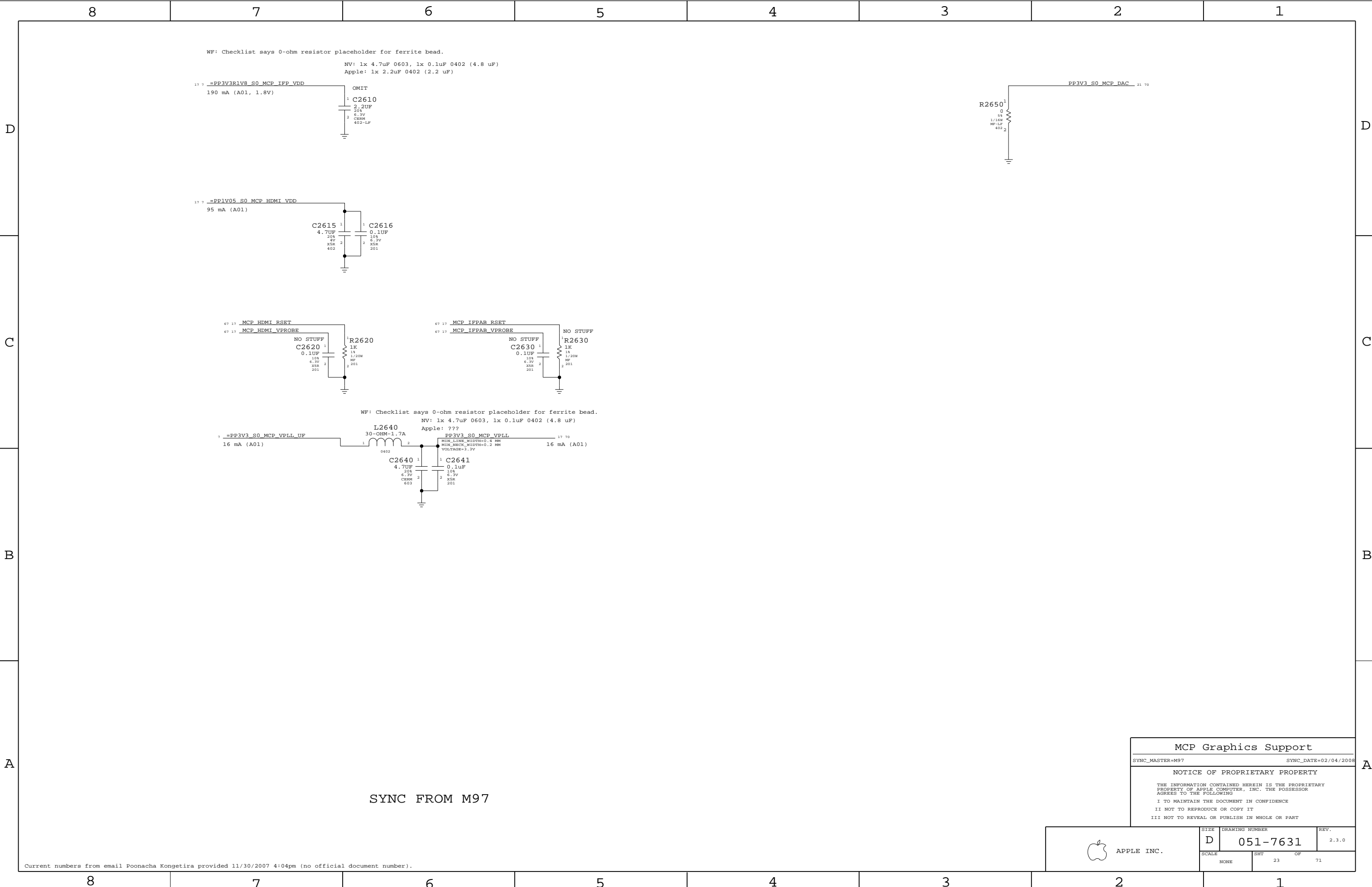
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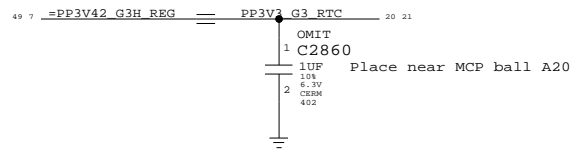
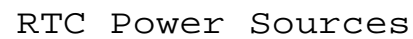
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SCALE	SHT	OF
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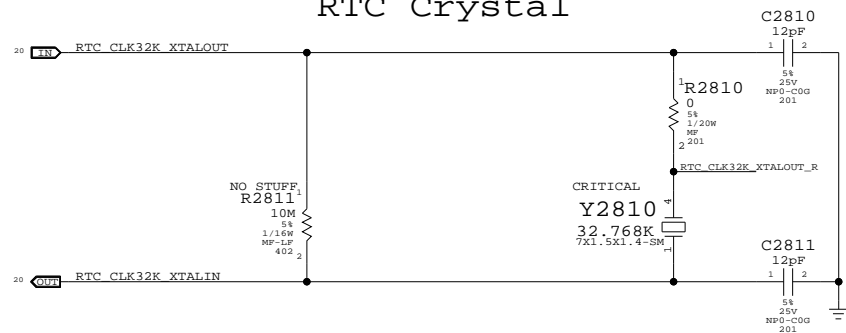
SYNC FROM M97

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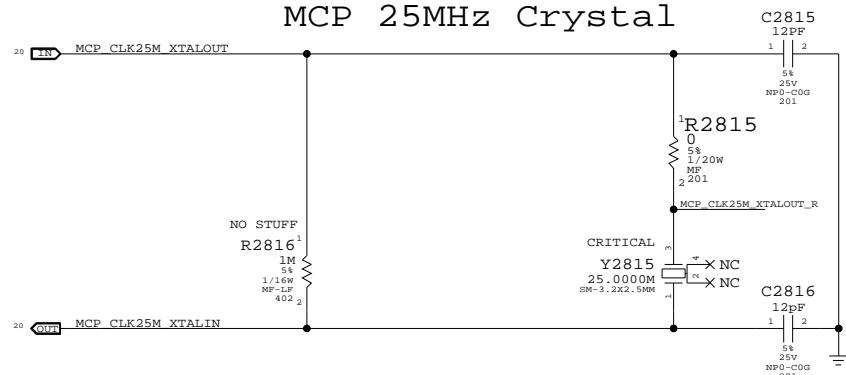
MCP Graphics Support			
SYNC_MASTER=M97		SYNC_DATE=02/04/2008	
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
	SCALE NONE	SHT 23	OF 71



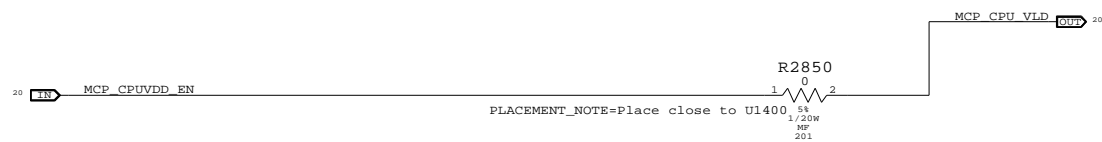
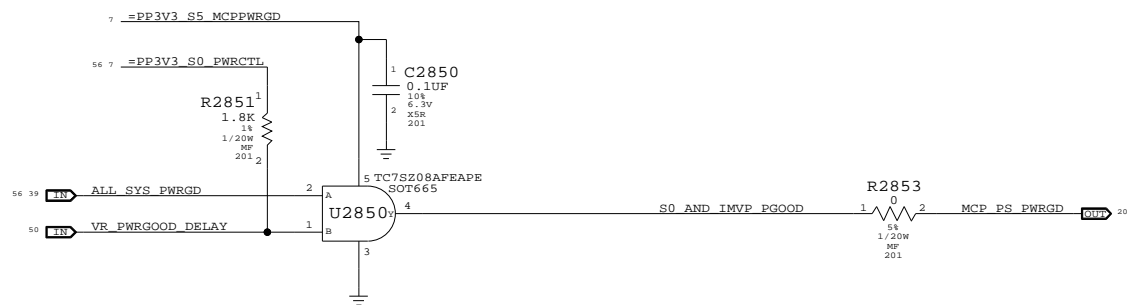
## RTC Crystal



## MCP 25MHz Crystal



## MCP S0 PWRGD &amp; CPU\_VLD



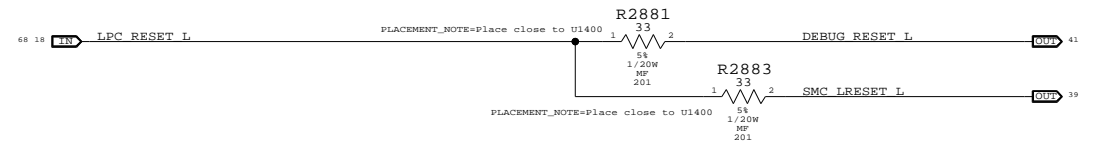
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SYNC FROM M97
CHANGED RTC POWER SOURCE TO DIRECT CONNECTION
ADDED MCPSEQ_SMC LOGIC

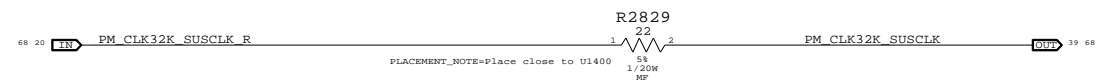
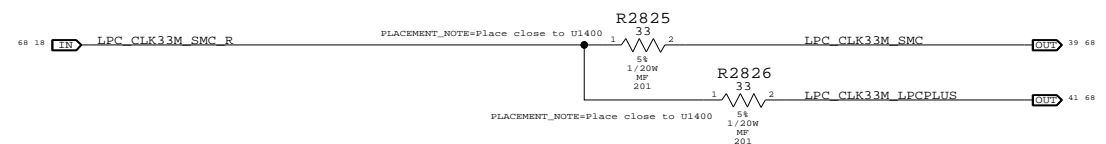
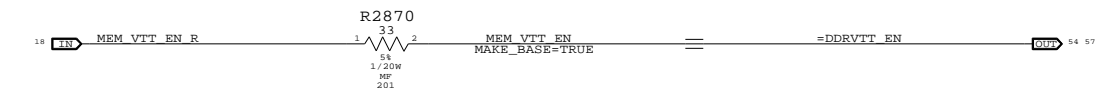
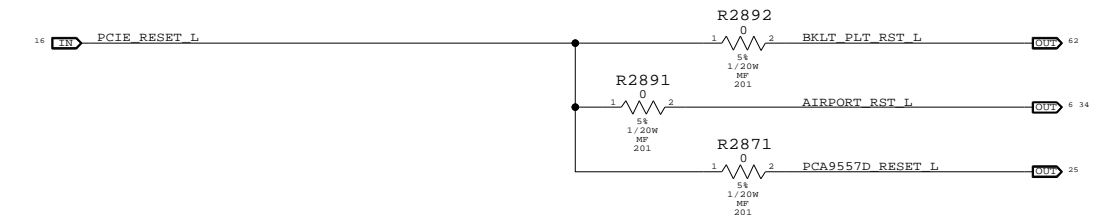
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## Platform Reset Connections

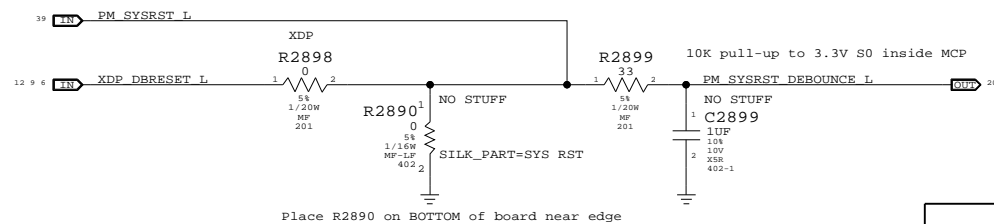
## LPC Reset (Unbuffered)



## PCIE Reset (Unbuffered)



## Reset Button



SB Misc			
SYNC_MASTER=M97		SYNC_DATE=02/04/2008	
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SCALE		SHT	OF
NONE		24	71



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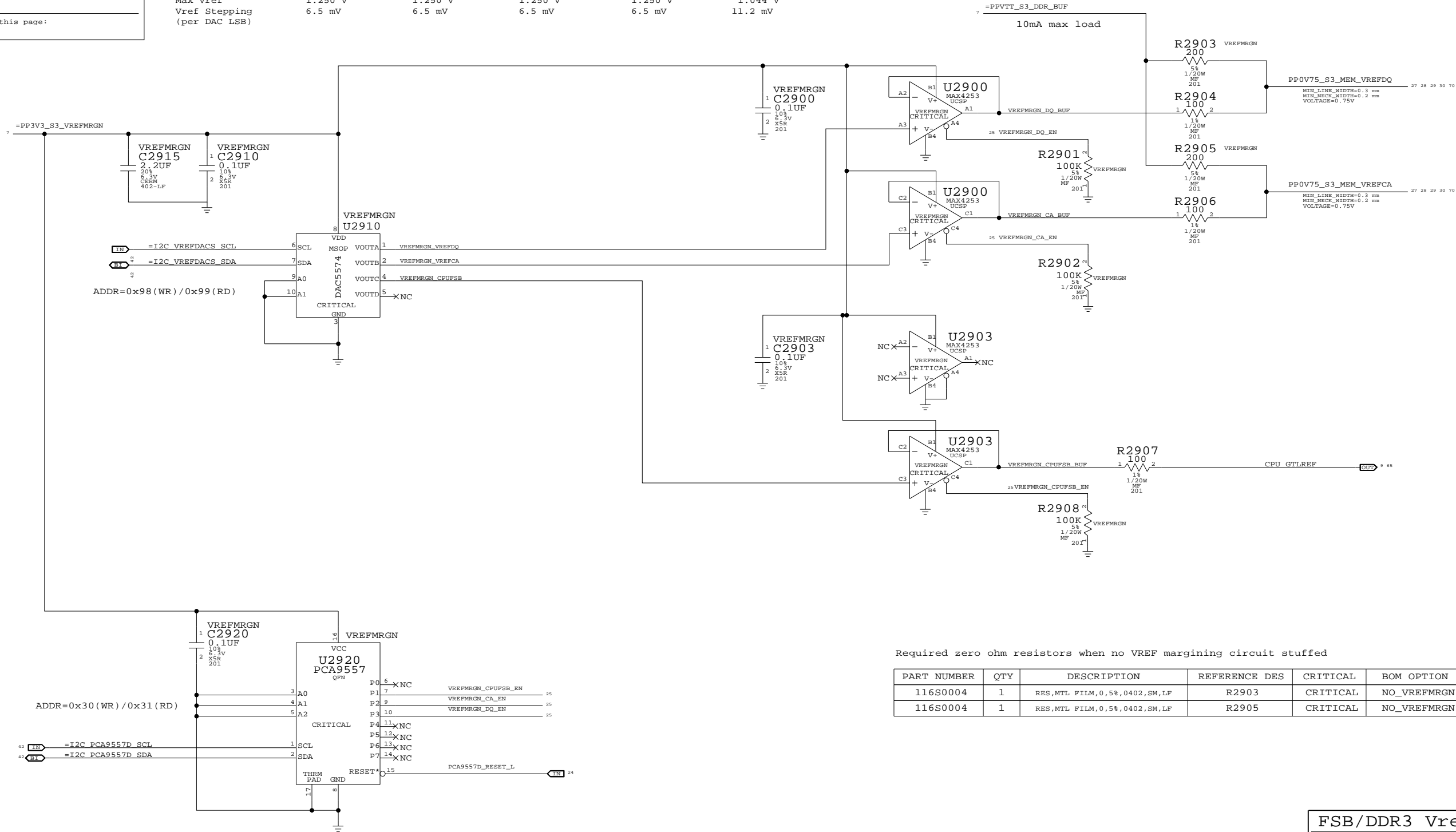
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- =PP3V3\_S5\_VREFMRGN  
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
- =I2C\_VREFDACS\_SCL  
- =I2C\_VREFDACS\_SDA  
- =I2C\_PCA9557D\_SCL  
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
VREFMRGN

DAC channel  
Min DAC code  
Max DAC code  
Max sink I  
Max source I  
Nominal Vref  
Min Vref  
Max Vref  
Vref Stepping  
(per DAC LSB)

MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
A	B	A	B	C
0x00	0x00	0x00	0x00	0x00
0x87	0x87	0x87	0x87	0x55
-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
5 mA	5 mA	5 mA	5 mA	0.52 mA
0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC\_MASTER=BEN SYNC\_DATE=01/15/2008

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	25	71

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



APPLE INC.

## DDR3 Support

SYNC\_MASTER=T18\_MLE

SYNC\_DATE=01/30/2008

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DO NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE
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D

WING NUMBER

051-7631

EV.

2.3.0

SCALE	NONE
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SHT
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1

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26

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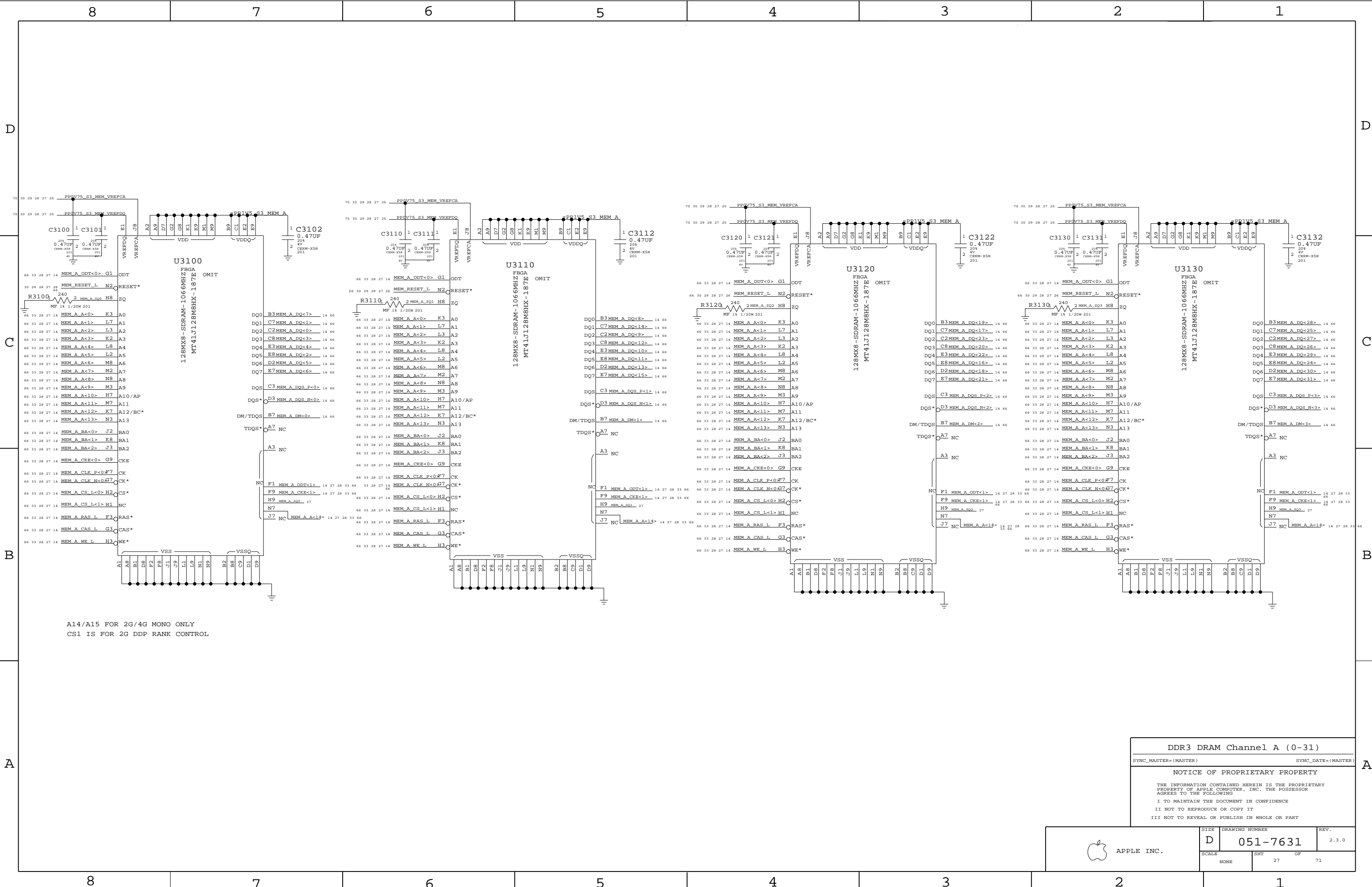
71

[illegible]

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DDR3 DRAM Channel A (0-31)

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

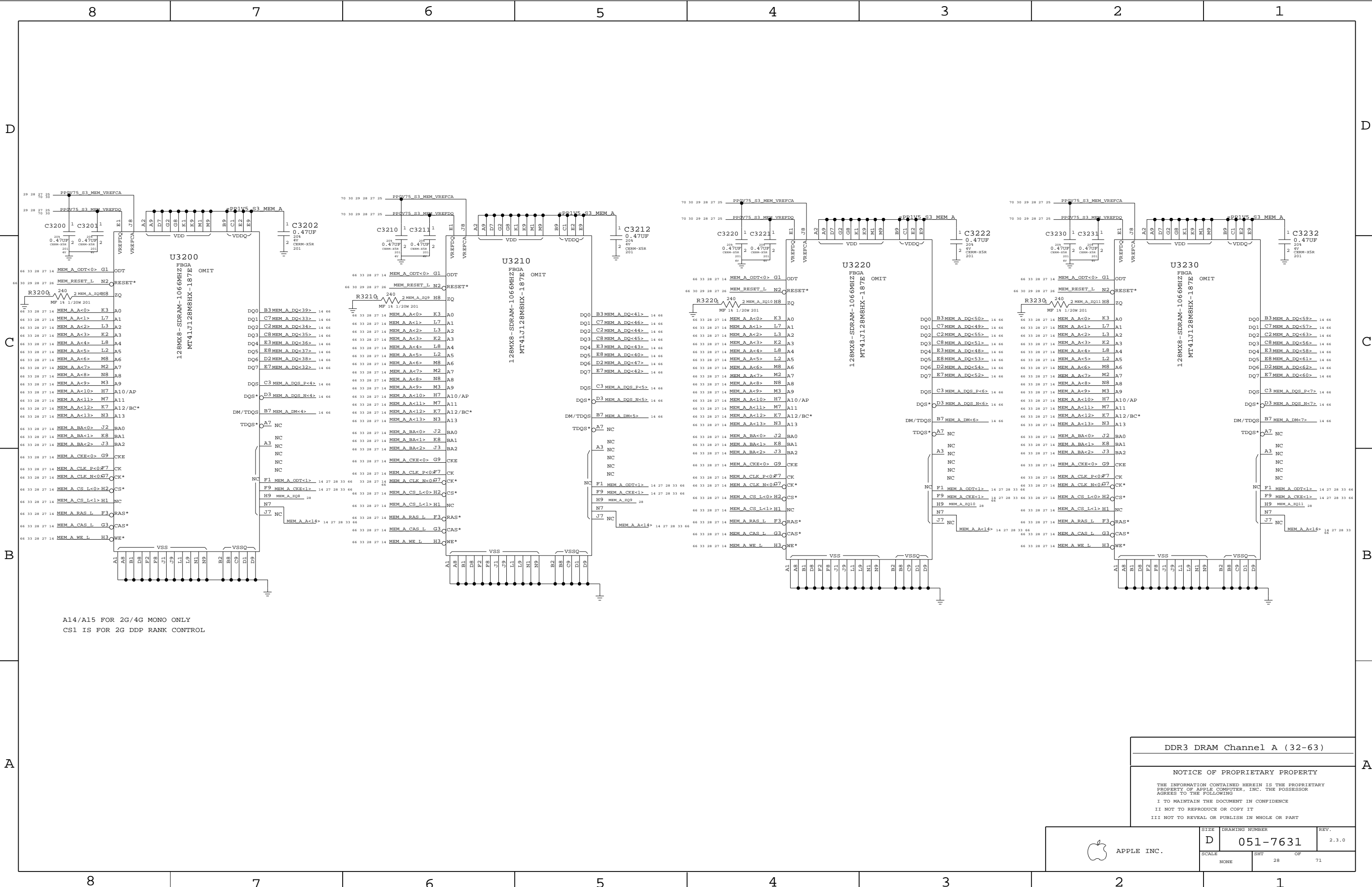
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A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel A (32-63)

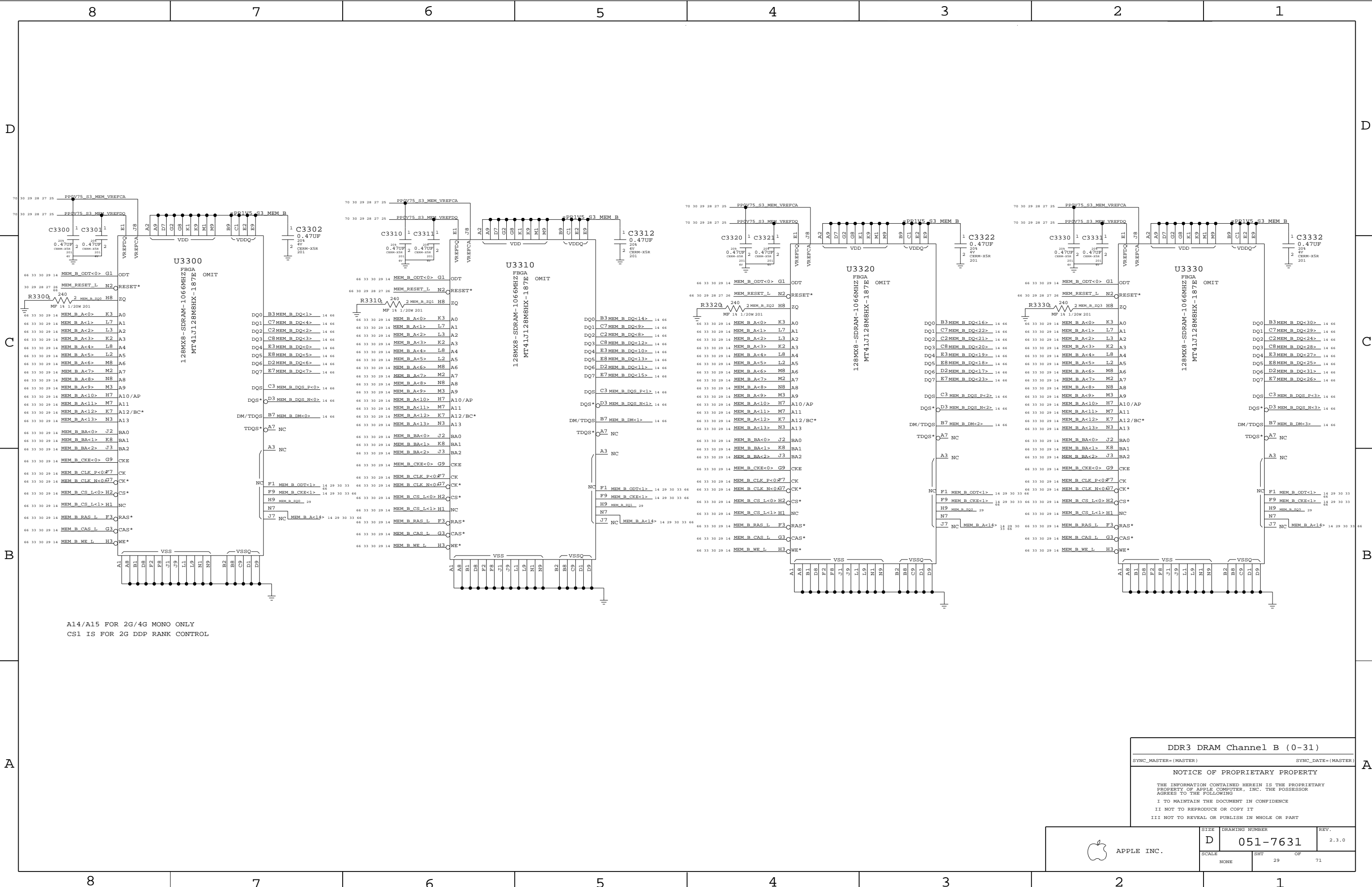
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A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel B (0-31)

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

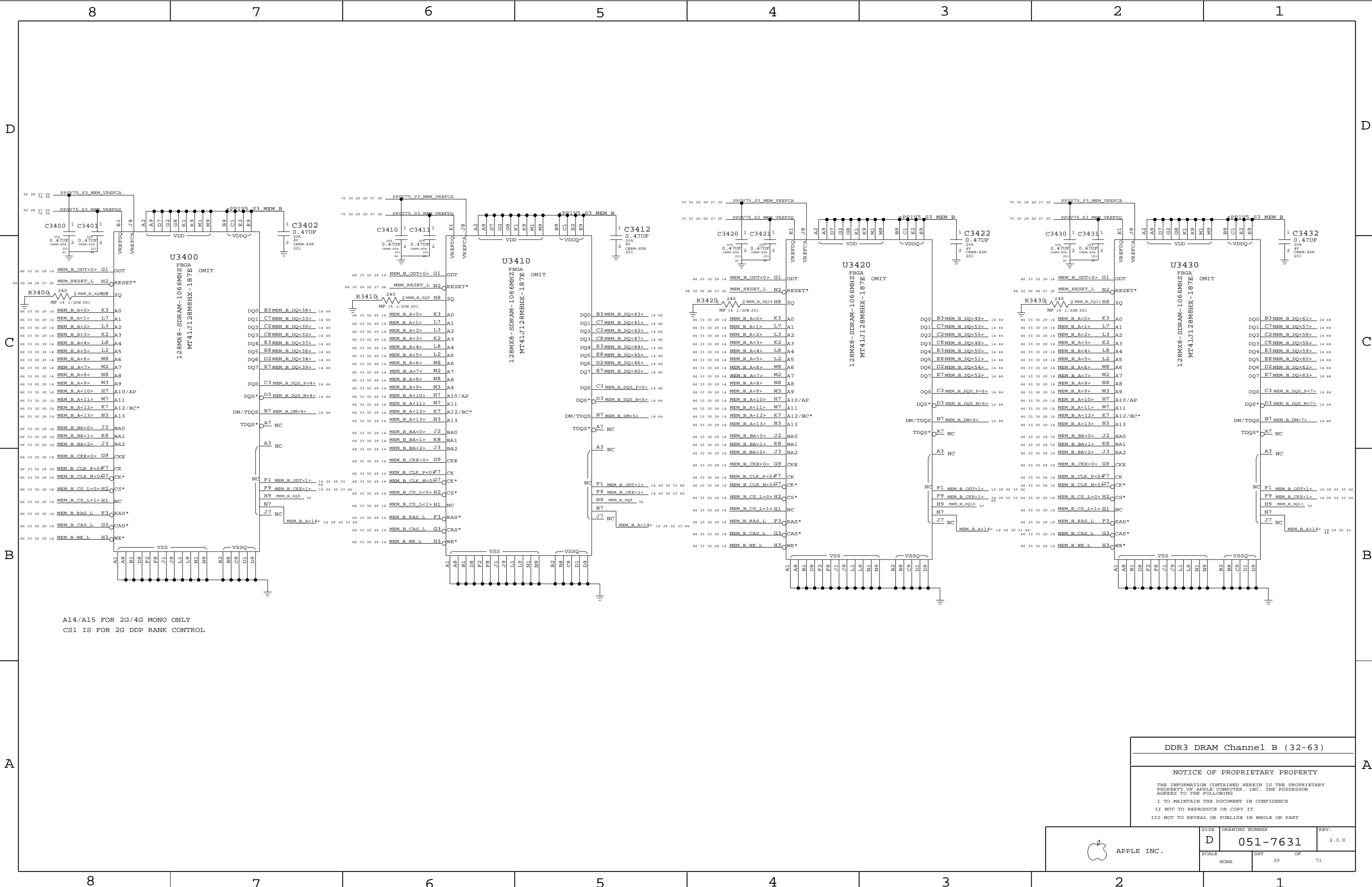
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CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel B (32-63)

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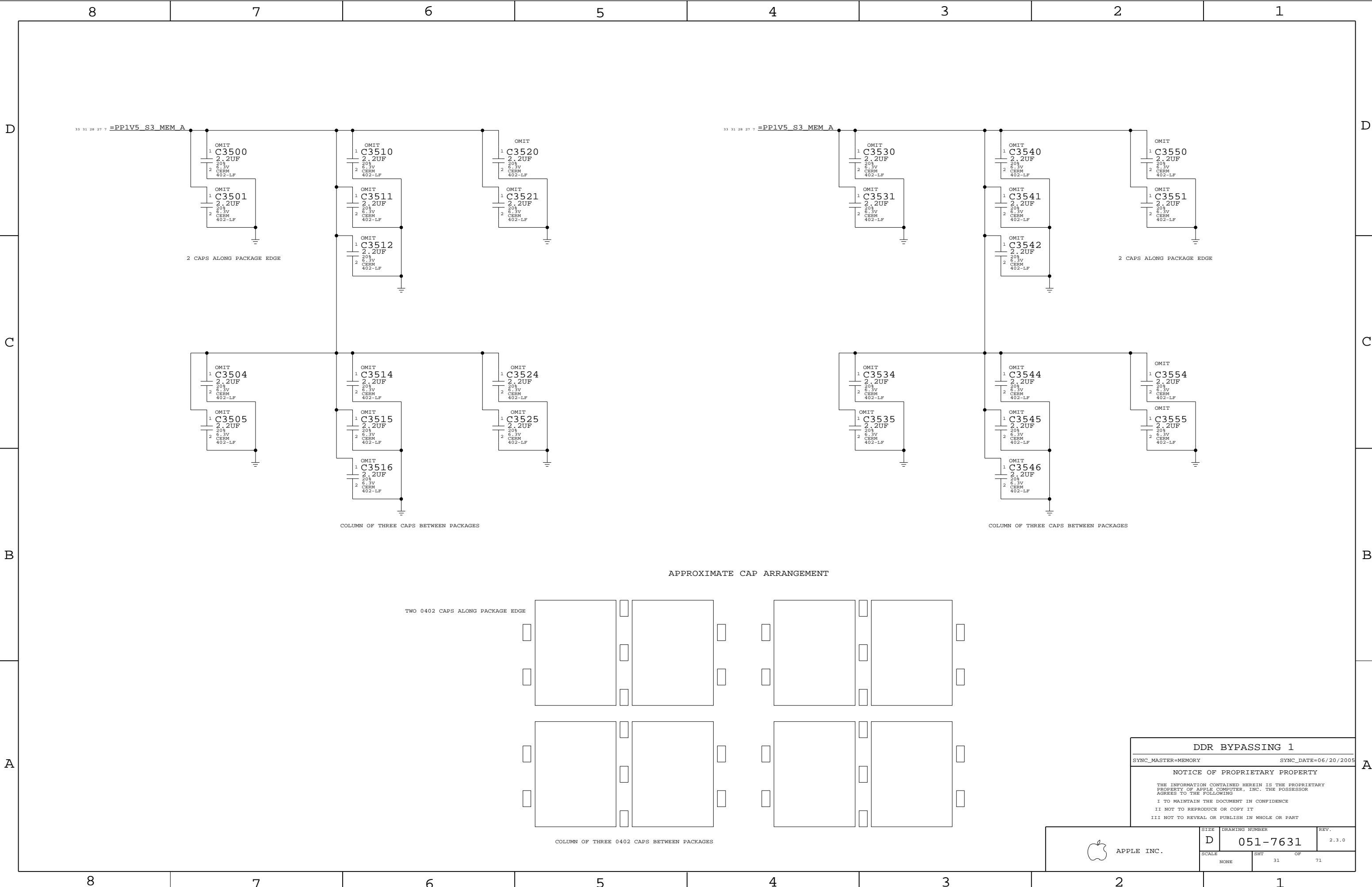
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	30	71



DDR BYPASSING 1

SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

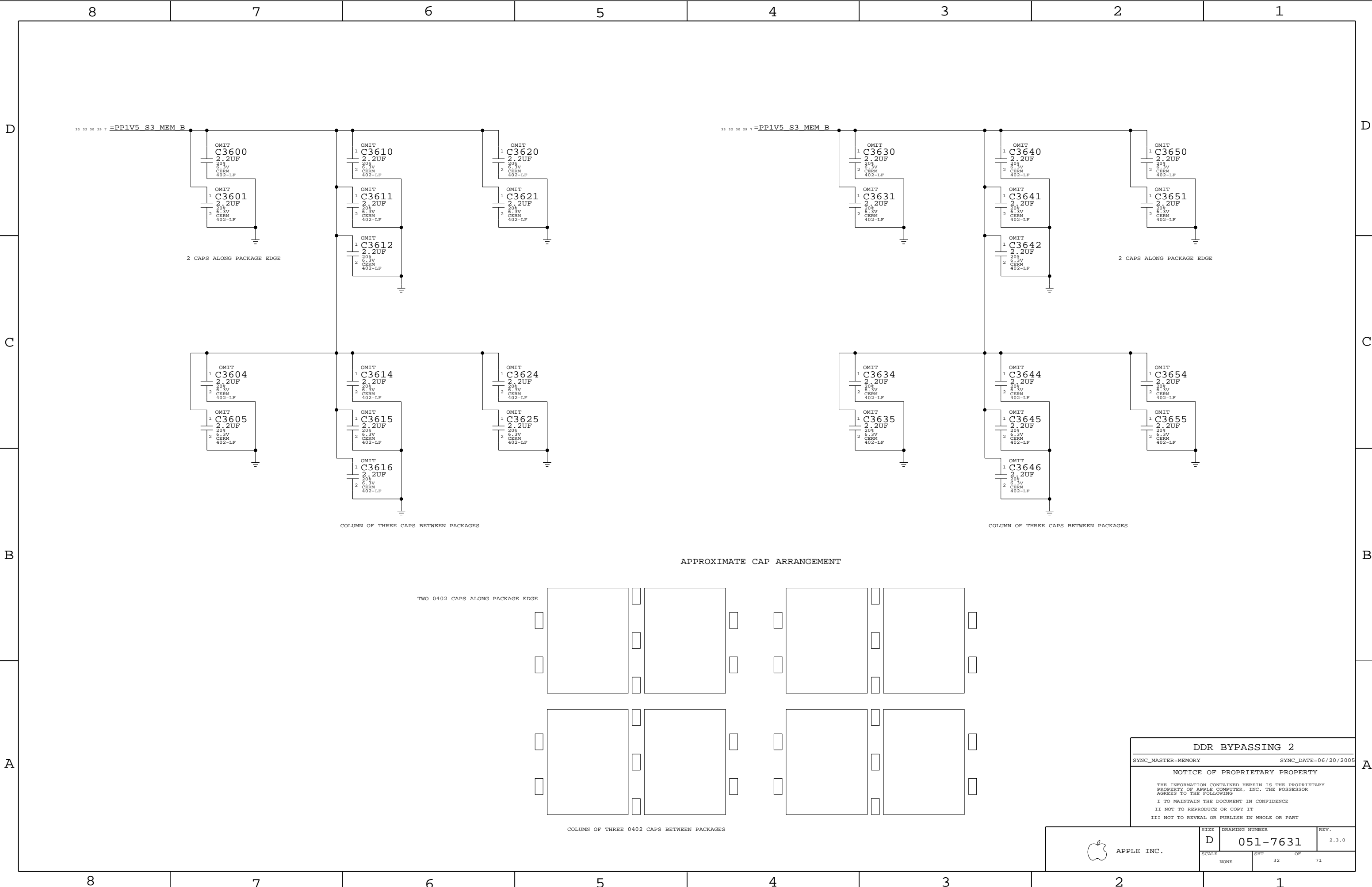
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE		SHT	OF
NONE		31	71



D

C

B

A

D

C

B

A

APPROXIMATE CAP ARRANGEMENT

DDR BYPASSING 2

SYNC\_MASTER=MEMORY

SYNC\_DATE=06/20/2005


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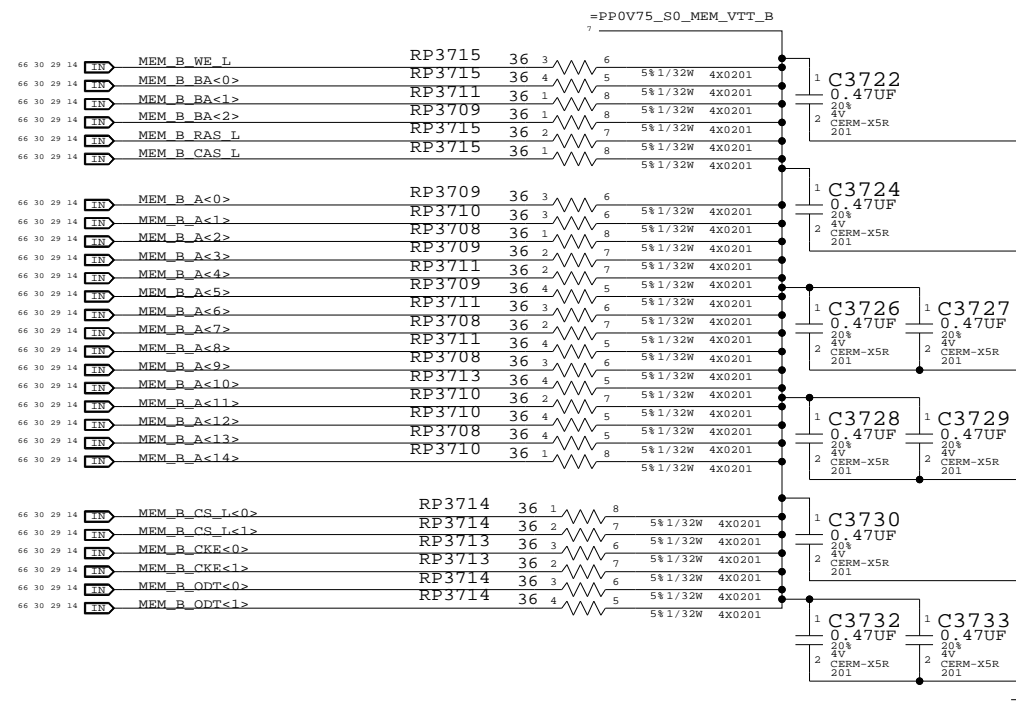
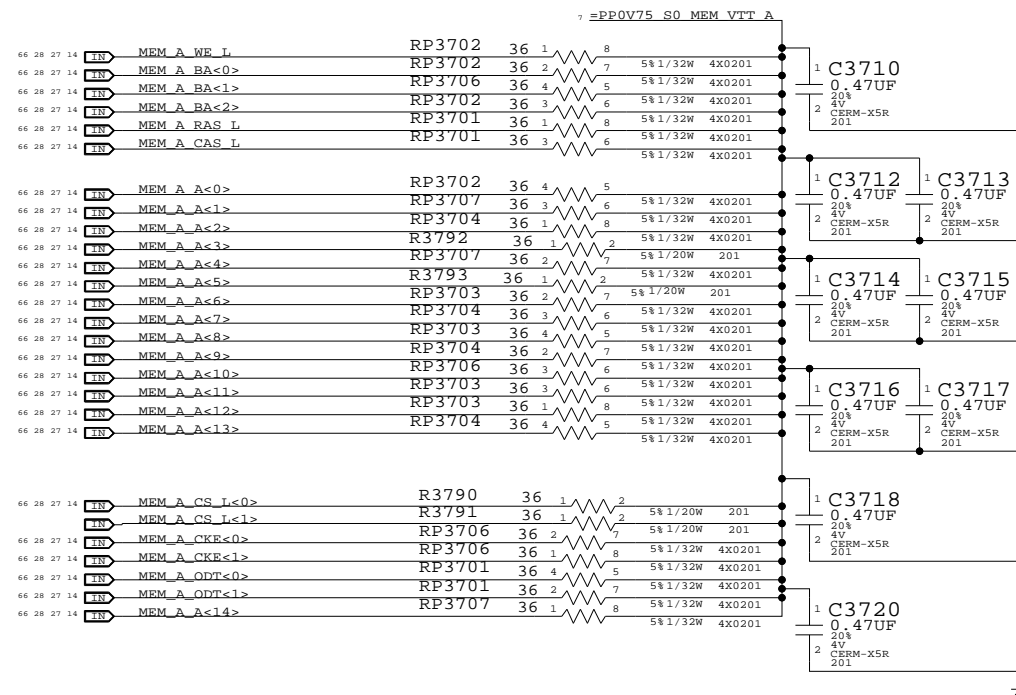
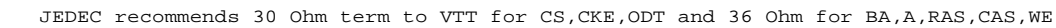
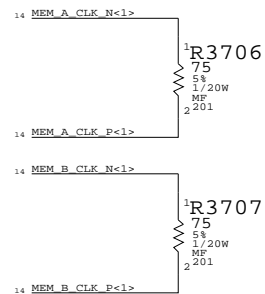
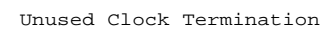
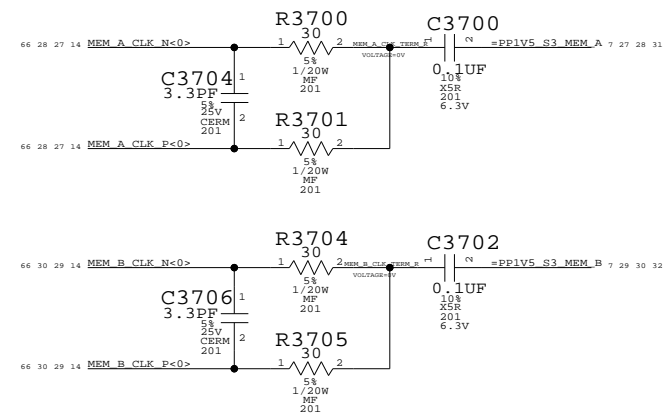
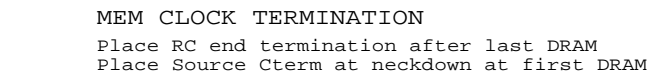
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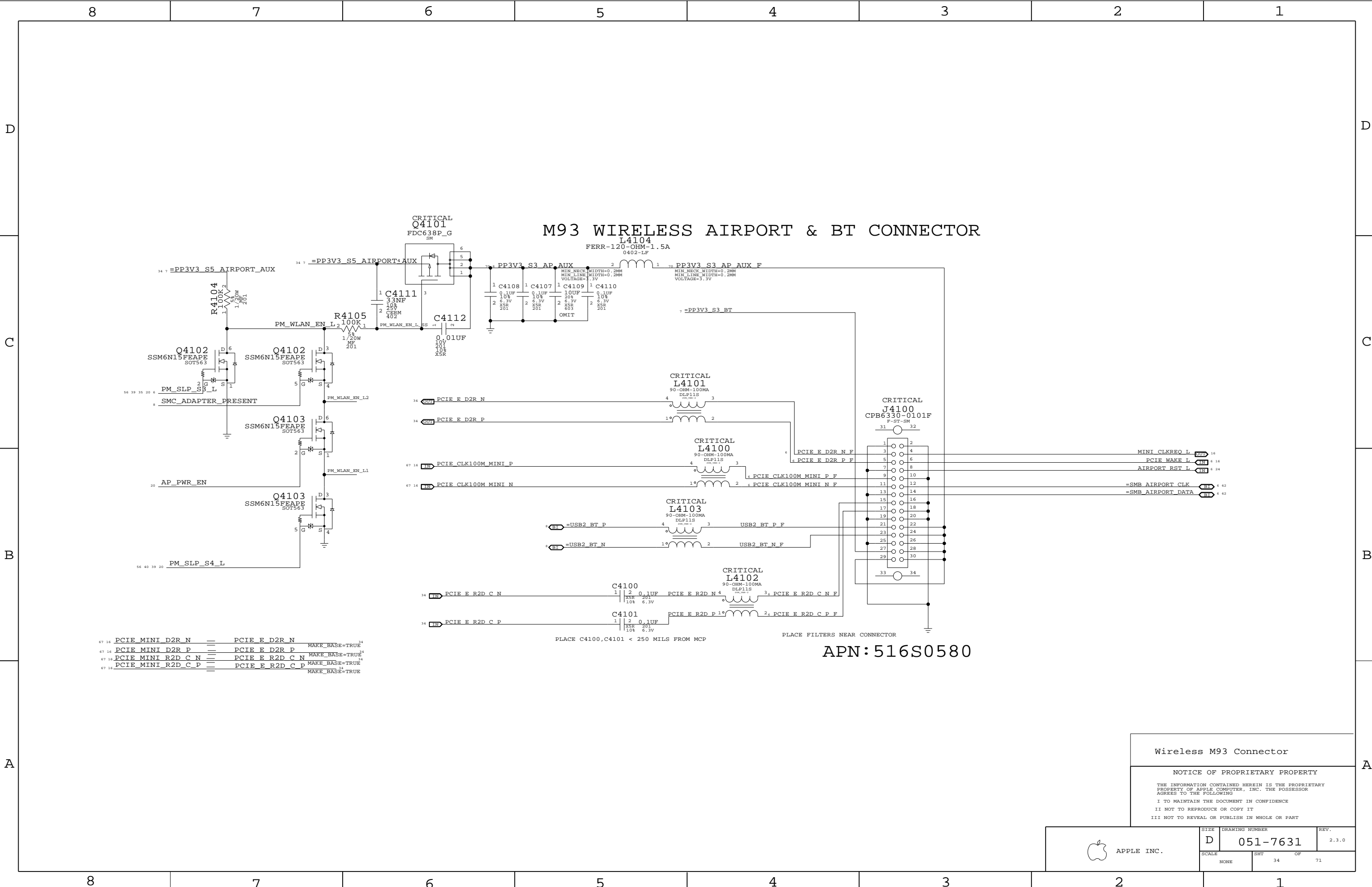
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7631		2.3.0
SCALE		SHT	OF	
NONE		32	71	



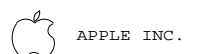




Wireless M93 Connector

NOTICE OF PROPRIETARY PROPERTY

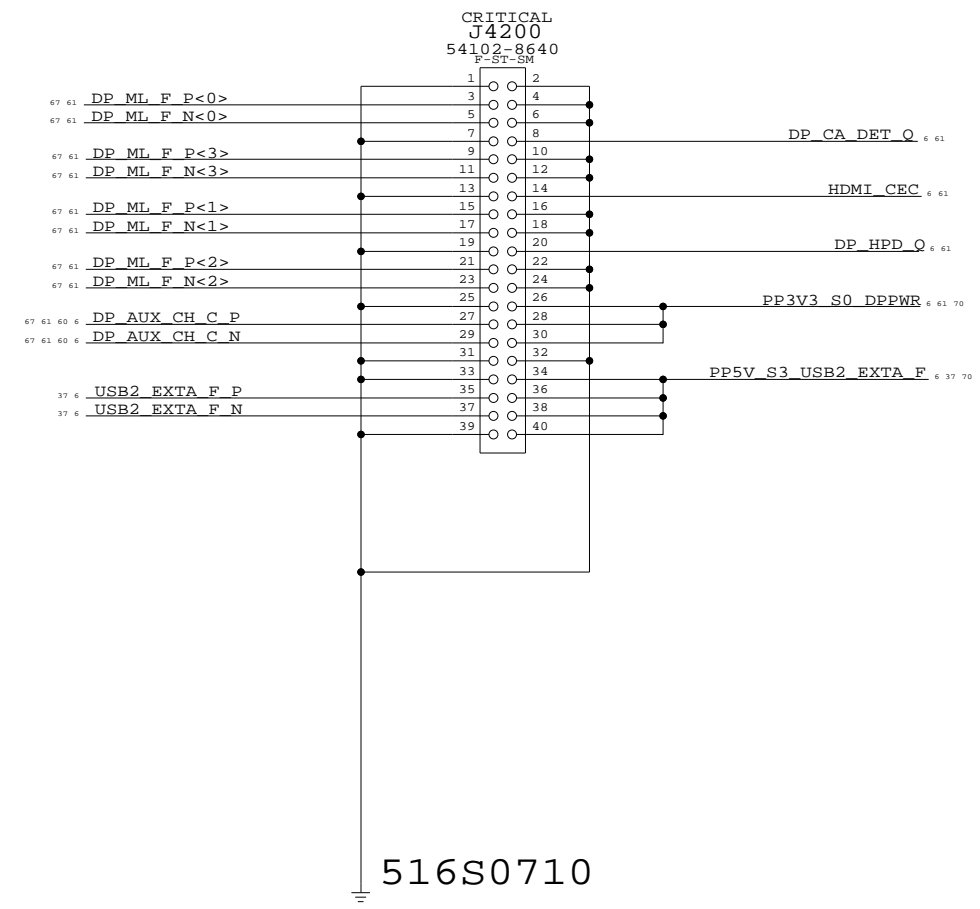
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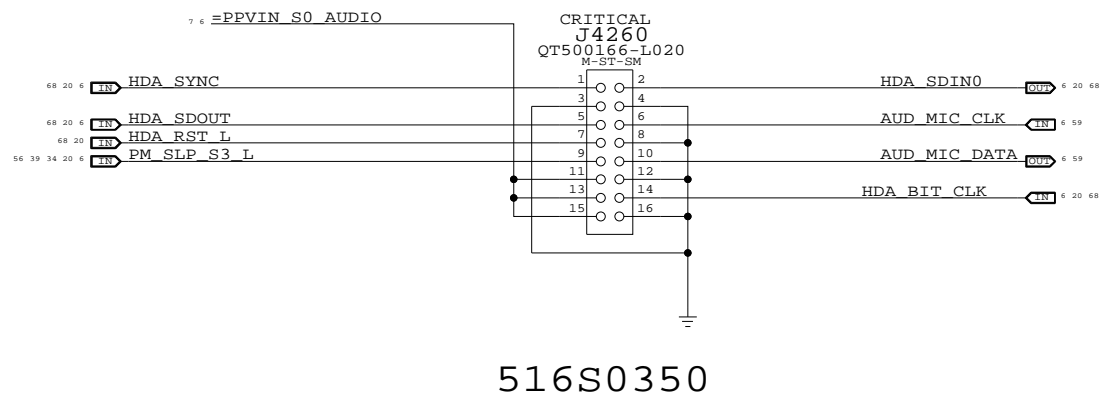
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	34	71

Micro-DisplayPort / USB to RIO Hatch Assembly



Audio Connector



Hatch and Audio Connectors

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)


NOTICE OF PROPRIETARY PROPERTY

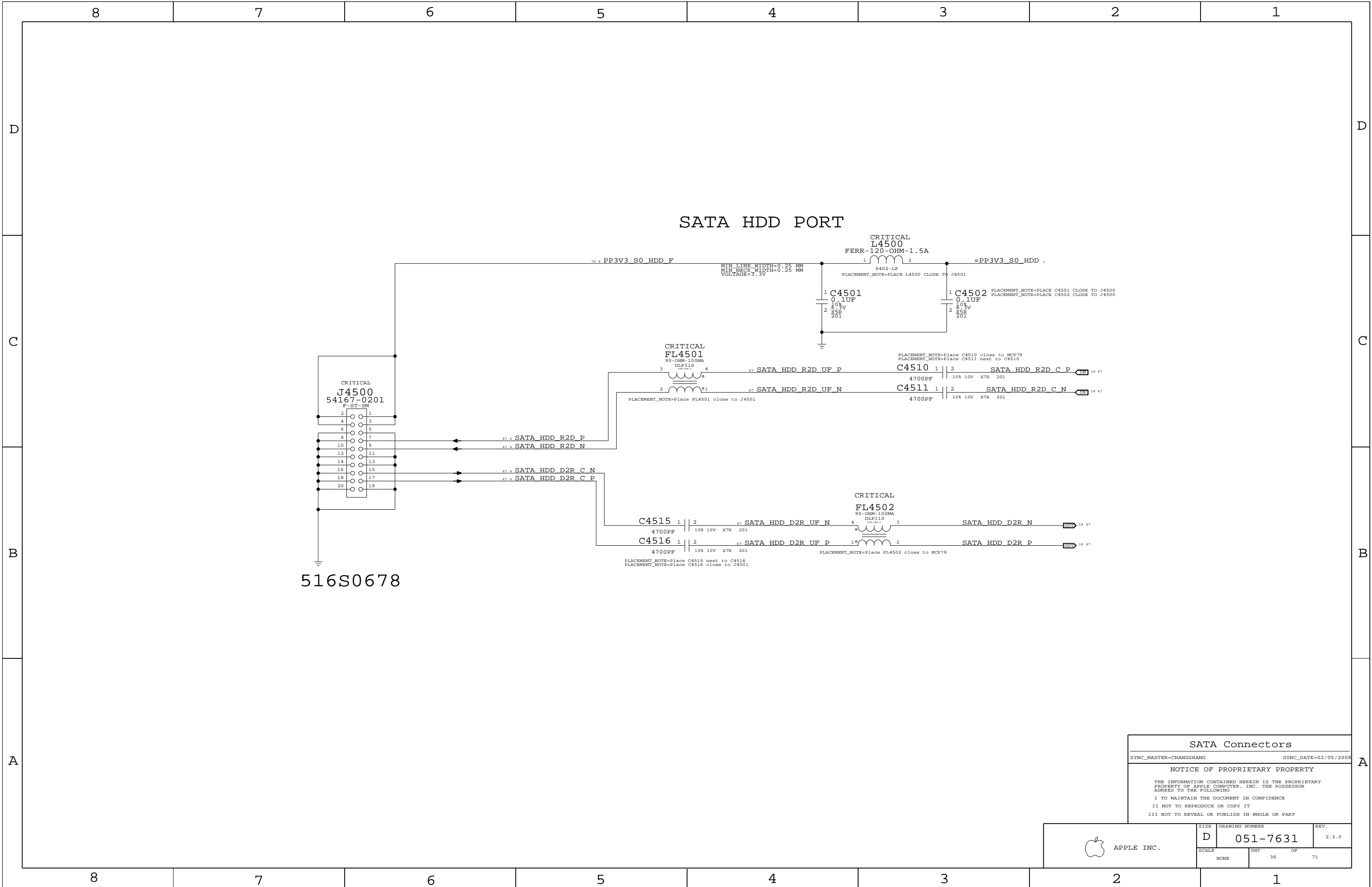
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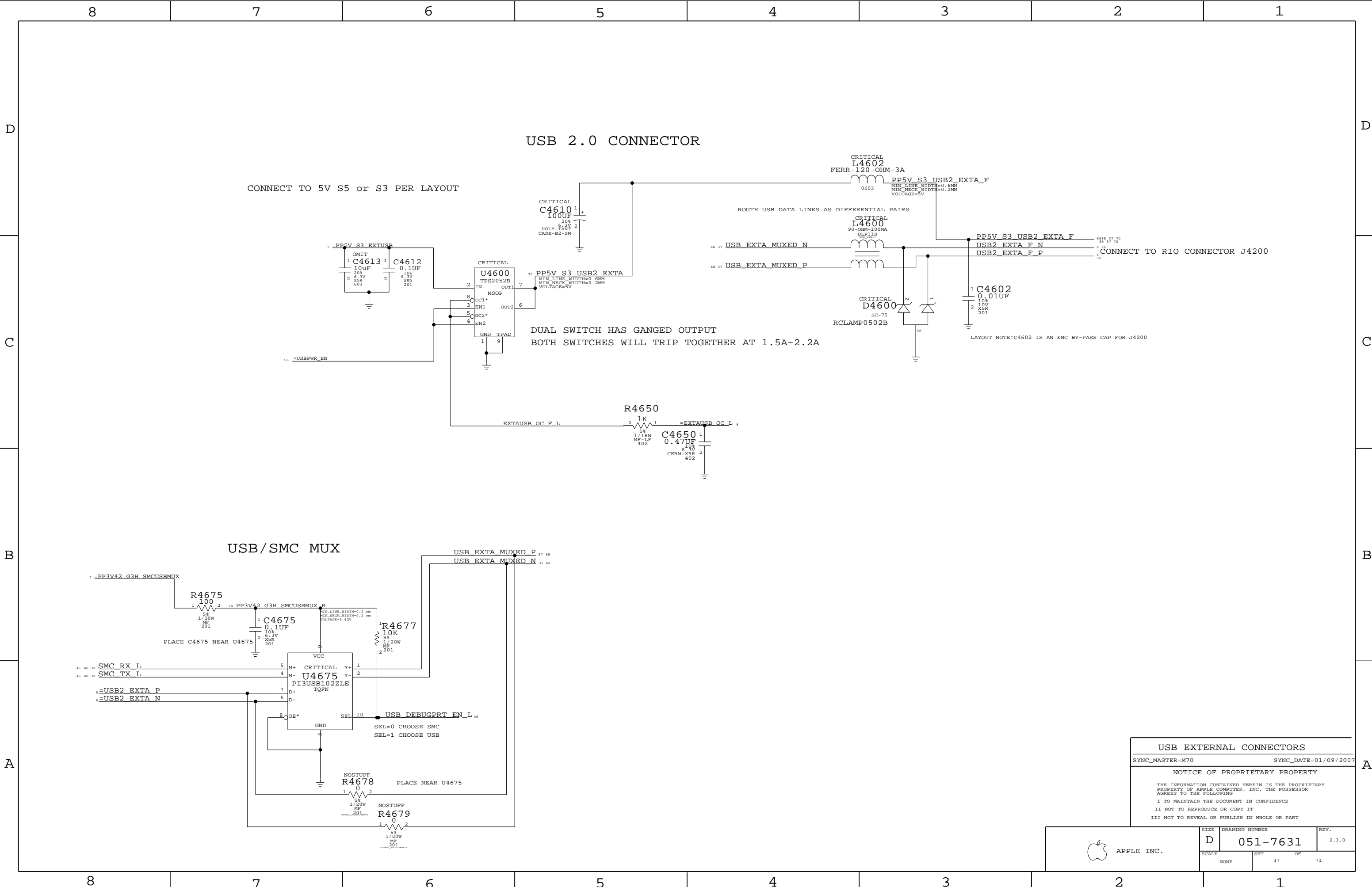
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7631		2.3.0
SCALE		SHT	OF	
NONE		35	71	





USB EXTERNAL CONNECTORS

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

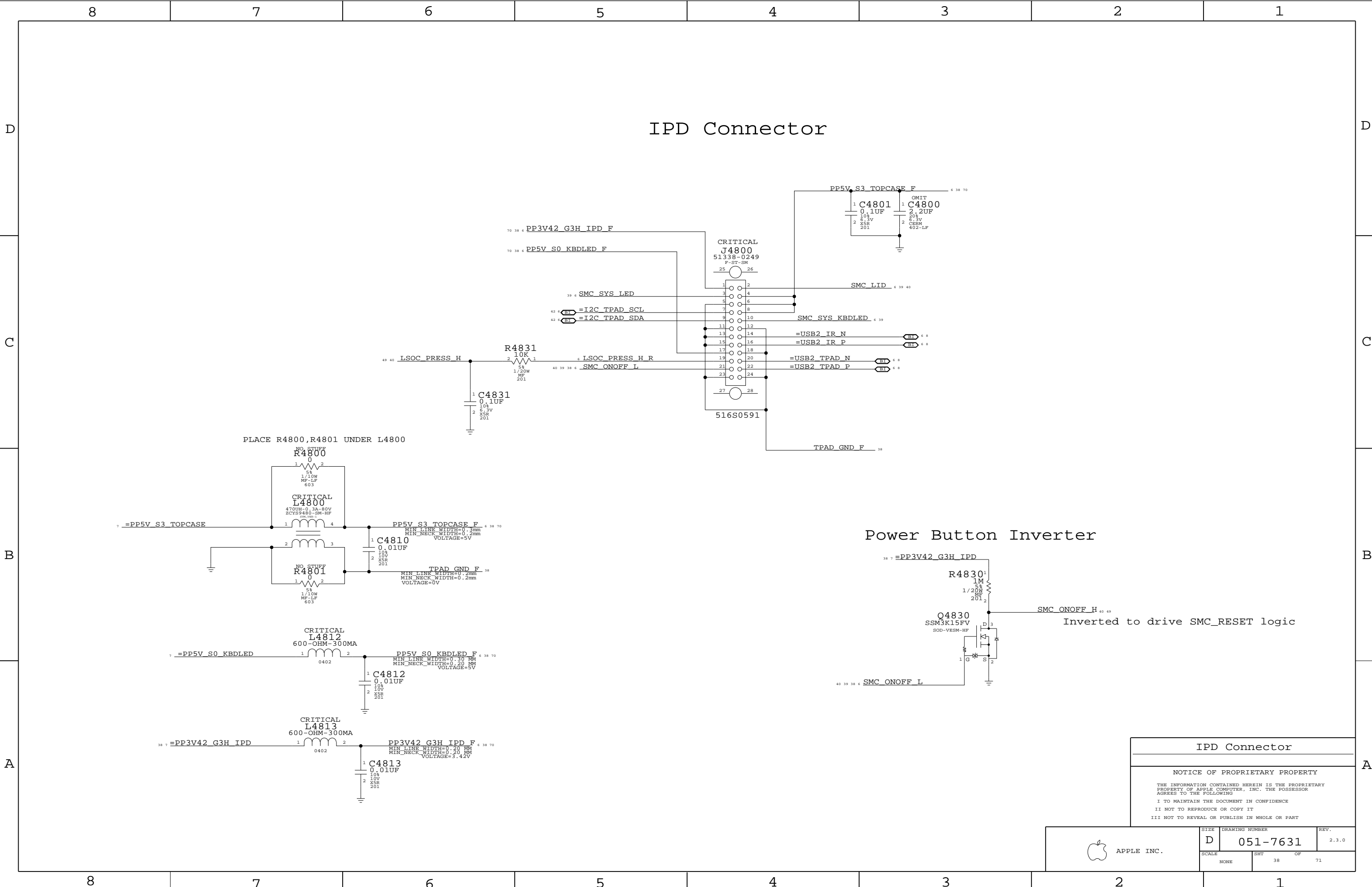
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING


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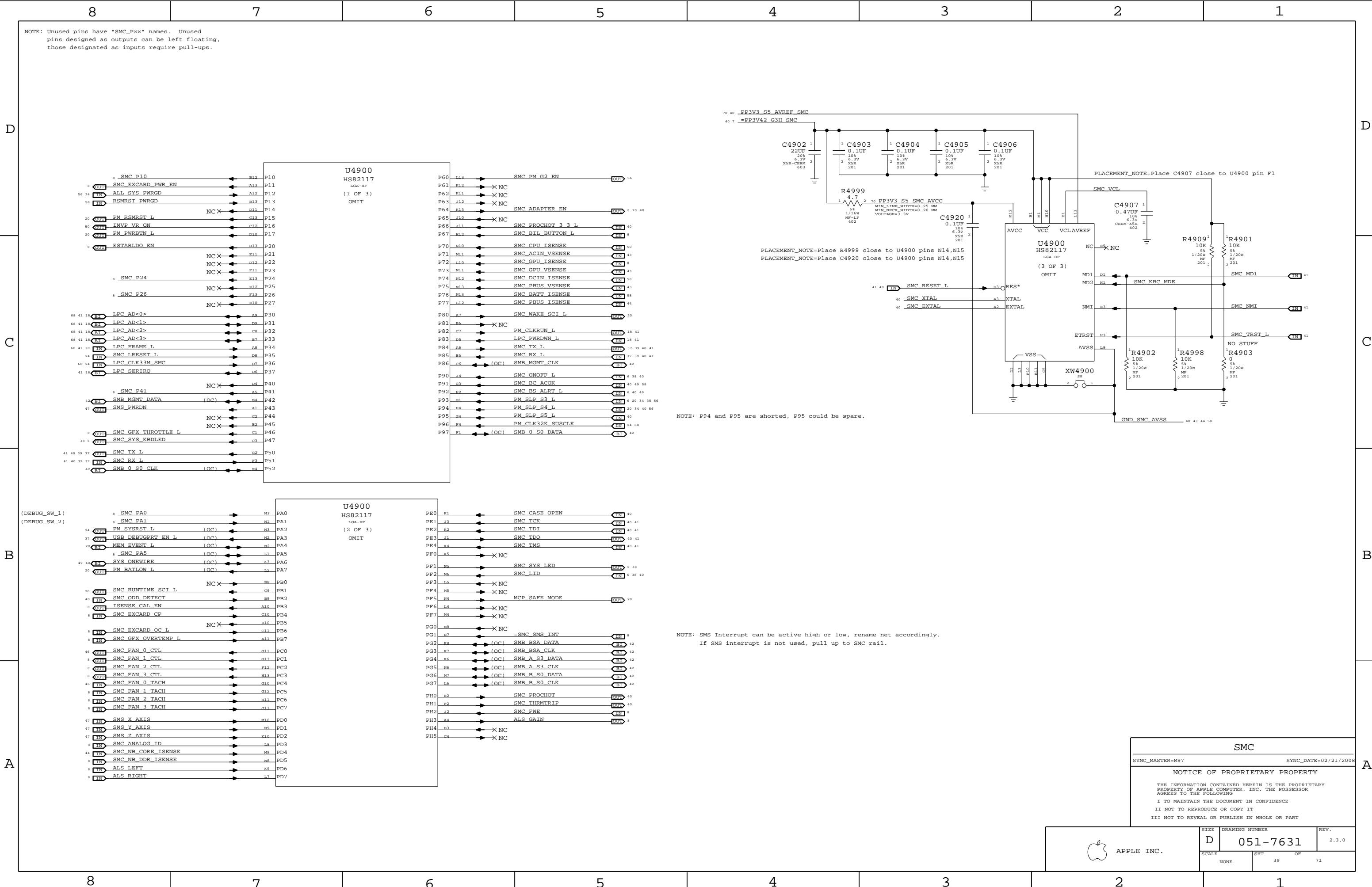
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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SCALE		SHT	OF
NONE		37	71

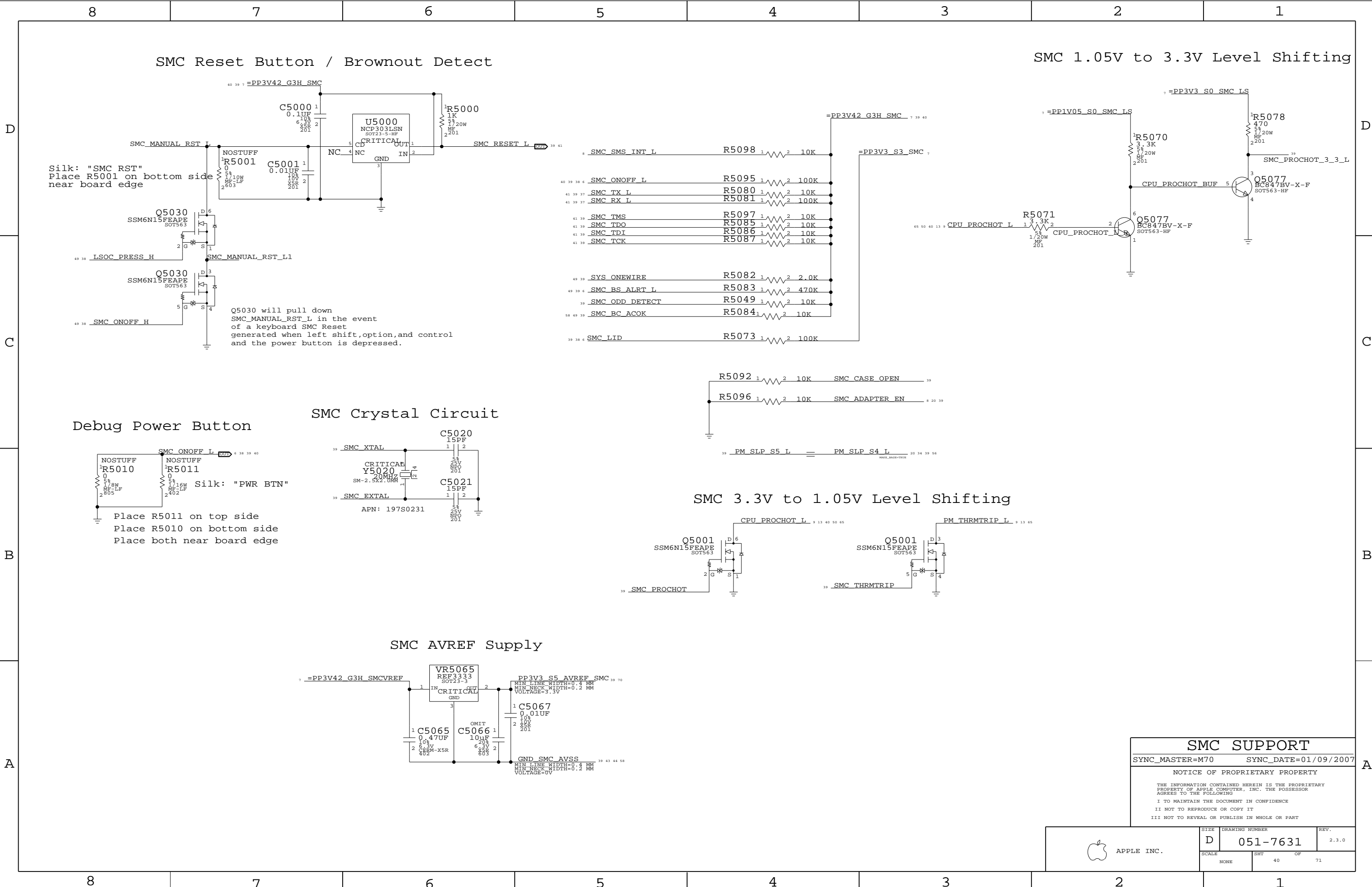


IPD Connector		
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
 APPLE INC.	SIZE	DRAWING NUMBER
	D	051-7631
SCALE	SHT	OF
NONE	38	71



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.  
If SMS interrupt is not used, pull up to SMC rail.



SMC Reset Button / Brownout Detect

SMC 1.05V to 3.3V Level Shifting

SMC Crystal Circuit

SMC 3.3V to 1.05V Level Shifting

SMC AVREF Supply

SMC SUPPORT

SYNC\_MASTER=M70

SYNC\_DATE=01/09/2007


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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	40	71



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

D



## C

B

## C

A



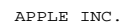
SYNC_MASTER=CHANGZHANG	SYNC_DATE=01/24/2008	7
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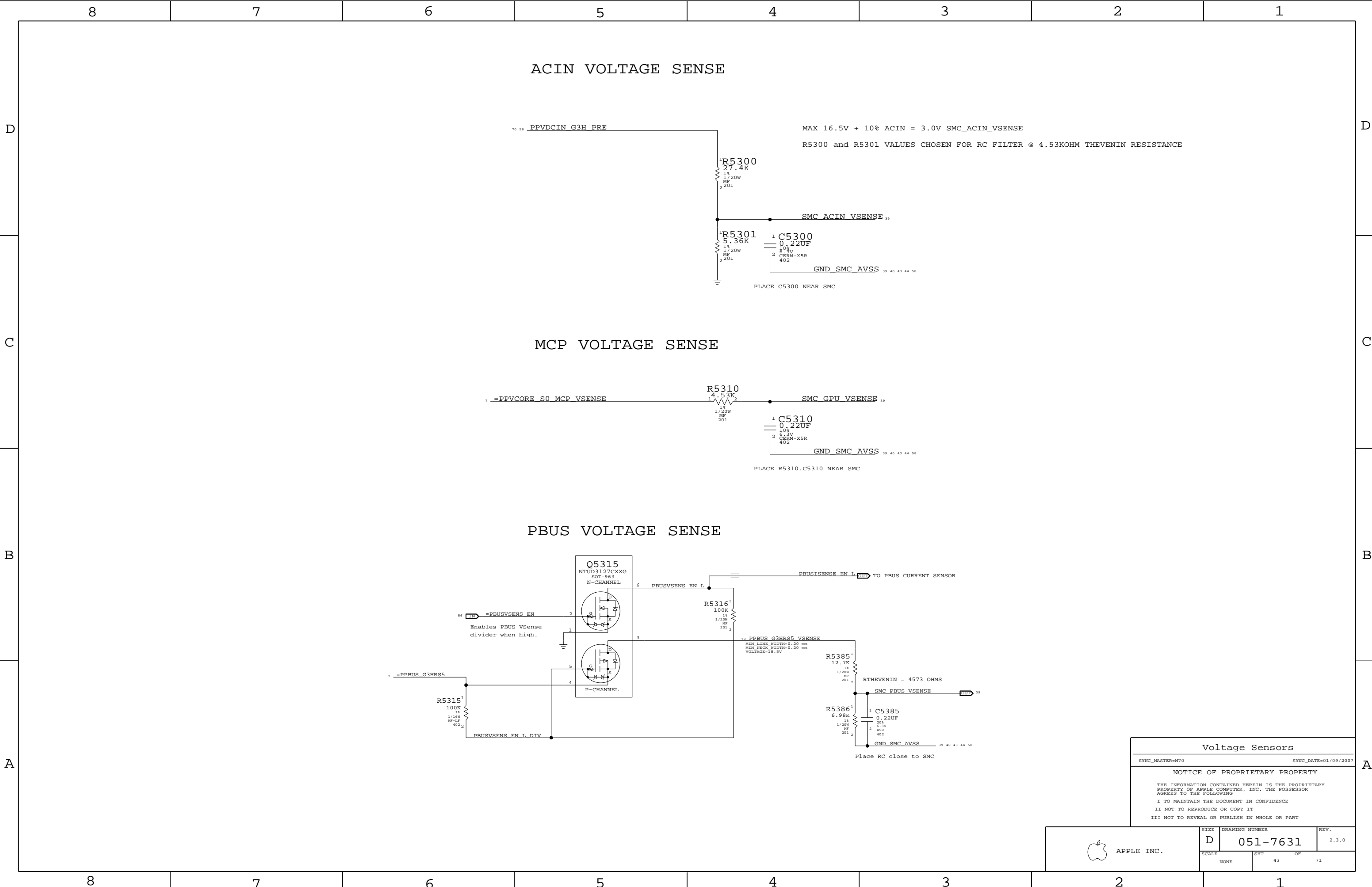
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



D	051-7631	2.3.0
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Voltage Sensors

SYNC\_MASTER=M70

SYNC\_DATE=01/09/2007


NOTICE OF PROPRIETARY PROPERTY

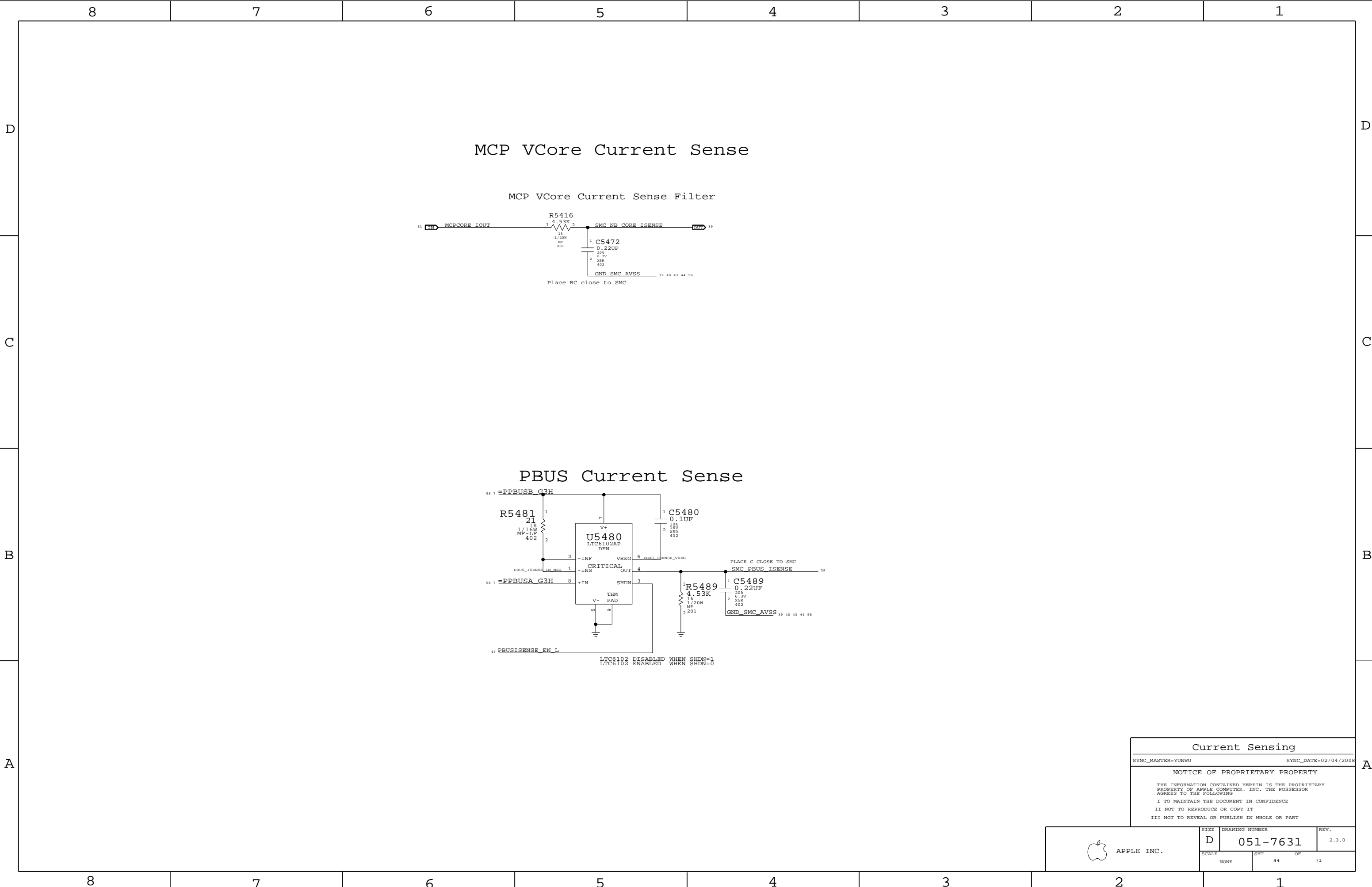
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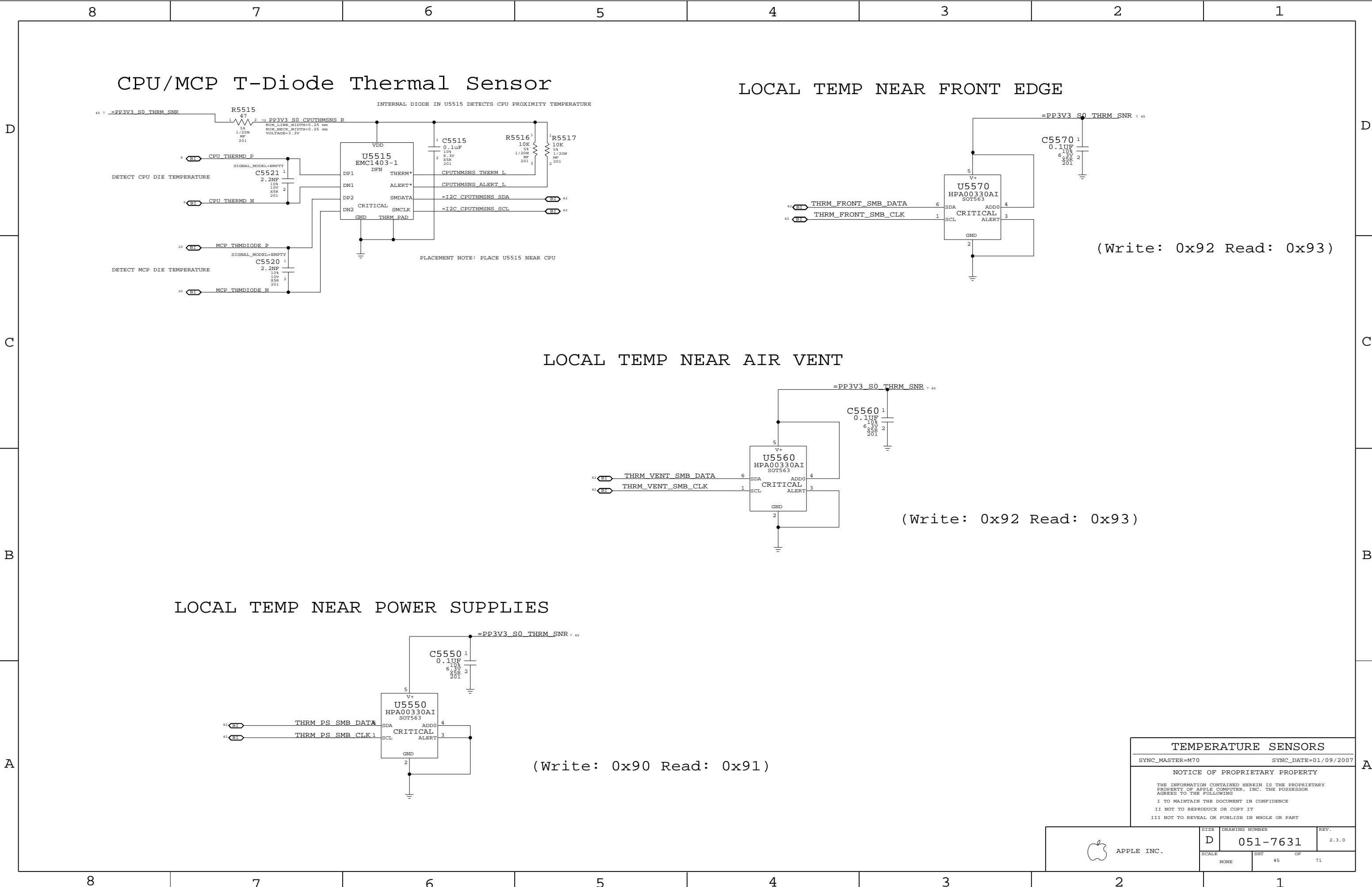
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
	SCALE NONE	SHT 43	OF 71






CPU/MCP T-Diode Thermal Sensor

LOCAL TEMP NEAR FRONT EDGE

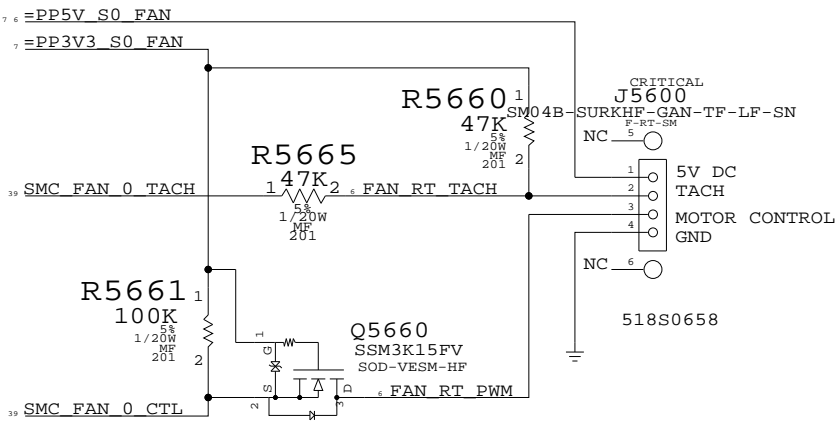
LOCAL TEMP NEAR AIR VENT

LOCAL TEMP NEAR POWER SUPPLIES

TEMPERATURE SENSORS		
SYNC_MASTER=M70		SYNC_DATE=01/09/2007
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE		SHT	OF
NONE		45	71

FAN CONNECTOR



Fan

SYNC\_MASTER=M70

SYNC\_DATE=01/09/2007


NOTICE OF PROPRIETARY PROPERTY

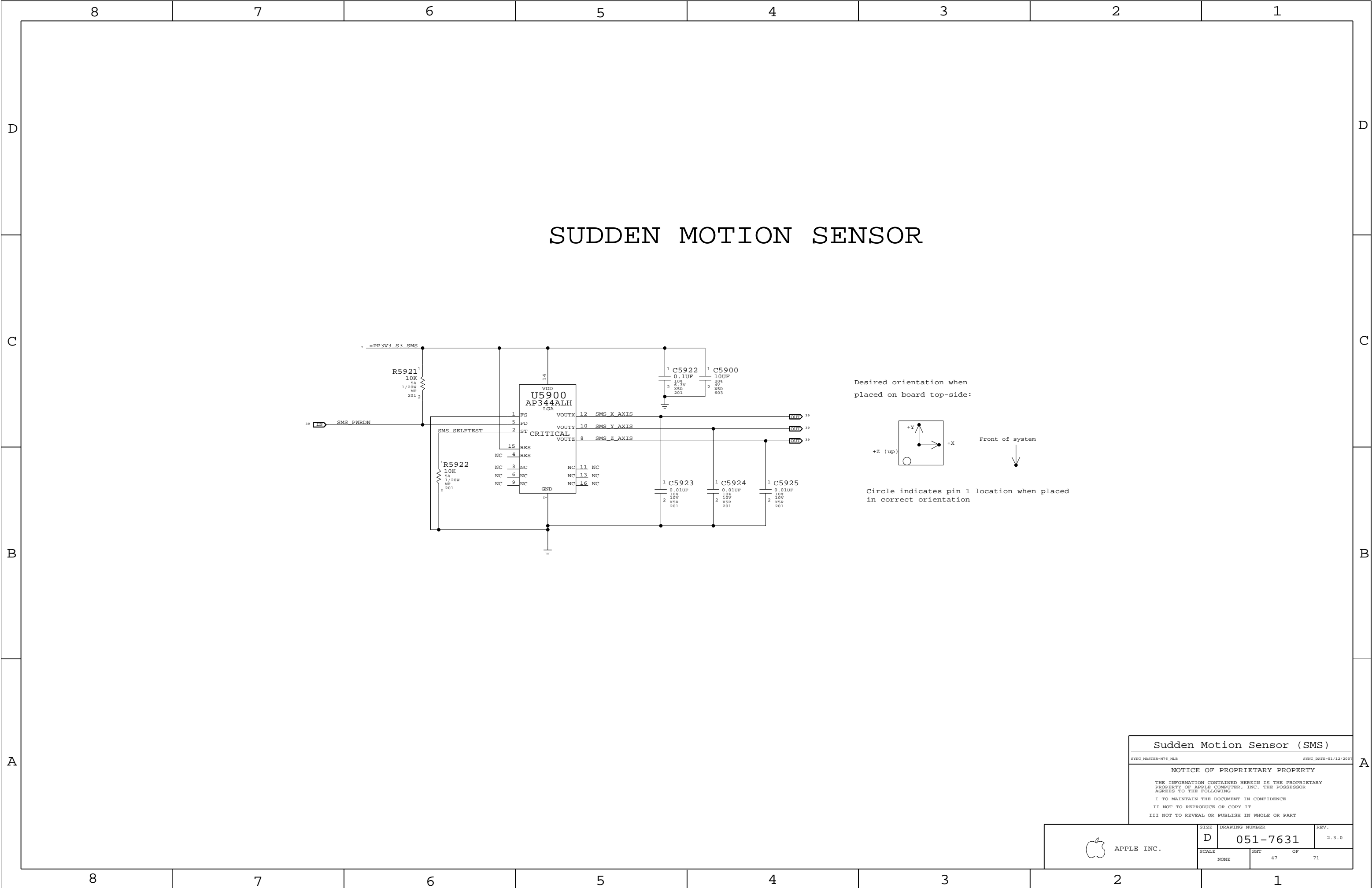
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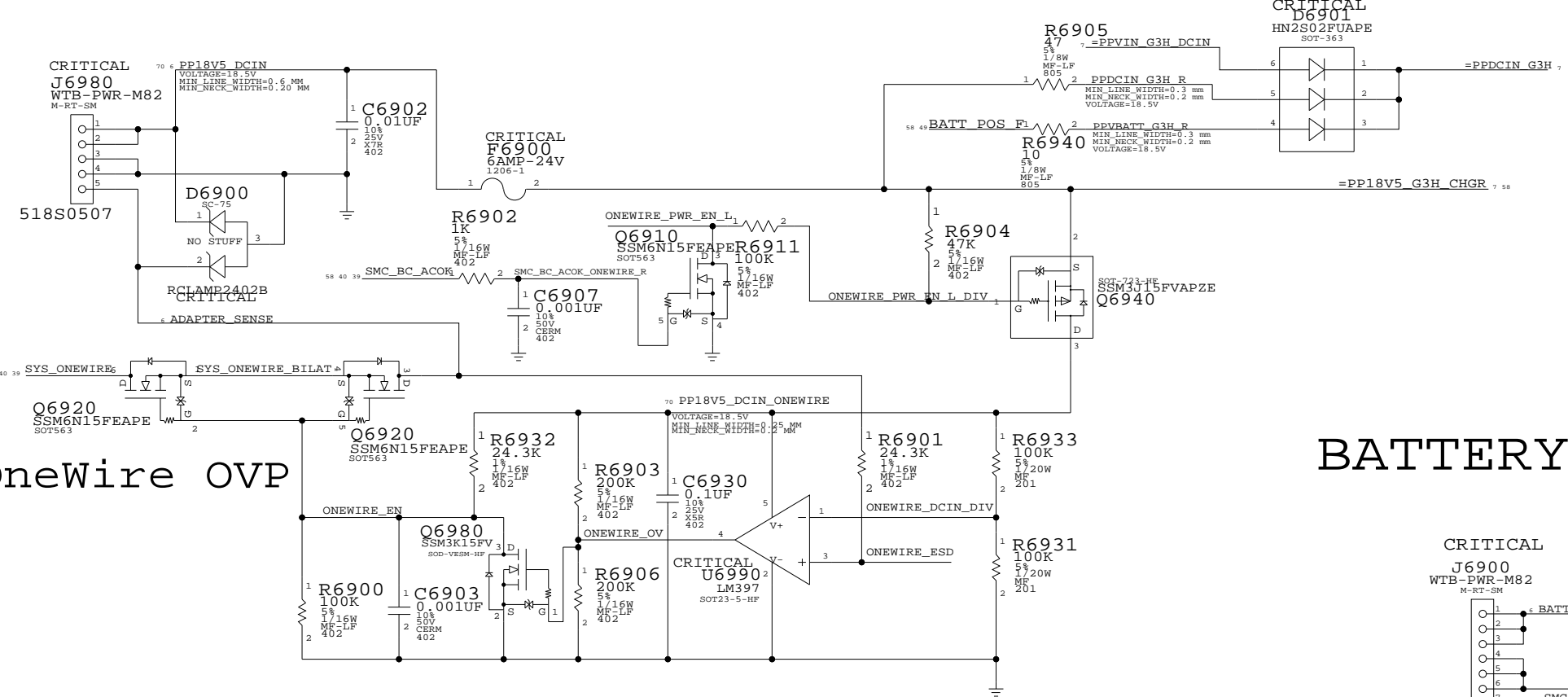
 APPLE INC.	SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
	SCALE NONE	SHT 46	OF 71



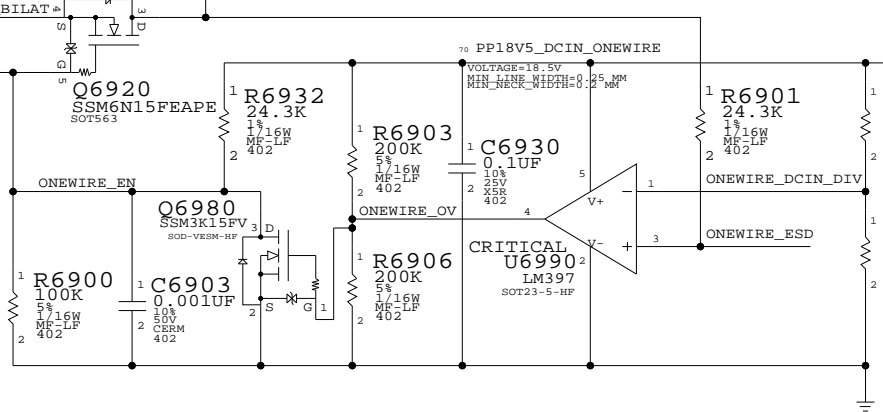




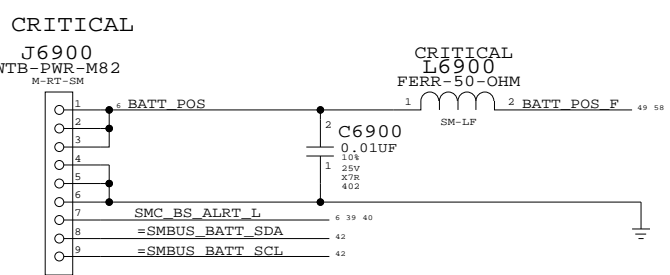
DC-JACK INTERFACE



OneWire OVP



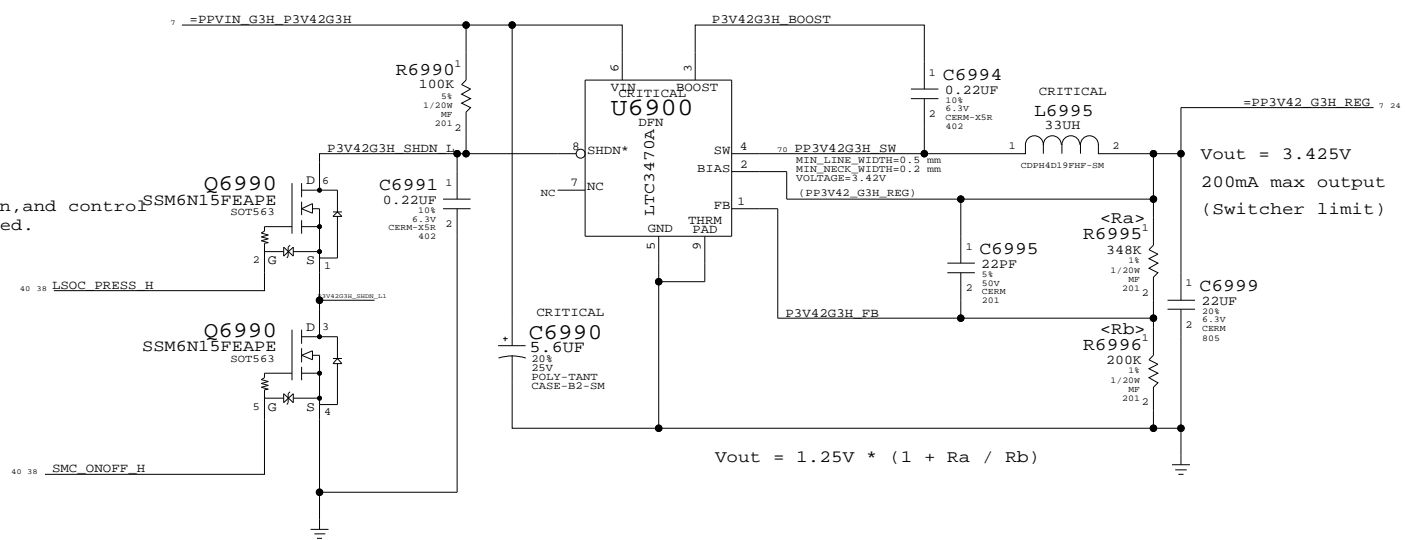
BATTERY INTERFACE



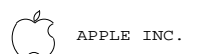
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Q6990 will pull down P3V42G3H\_SHDN\_L in the event of a keyboard SMC Reset generated when left shift,option,and control and the power button is depressed.



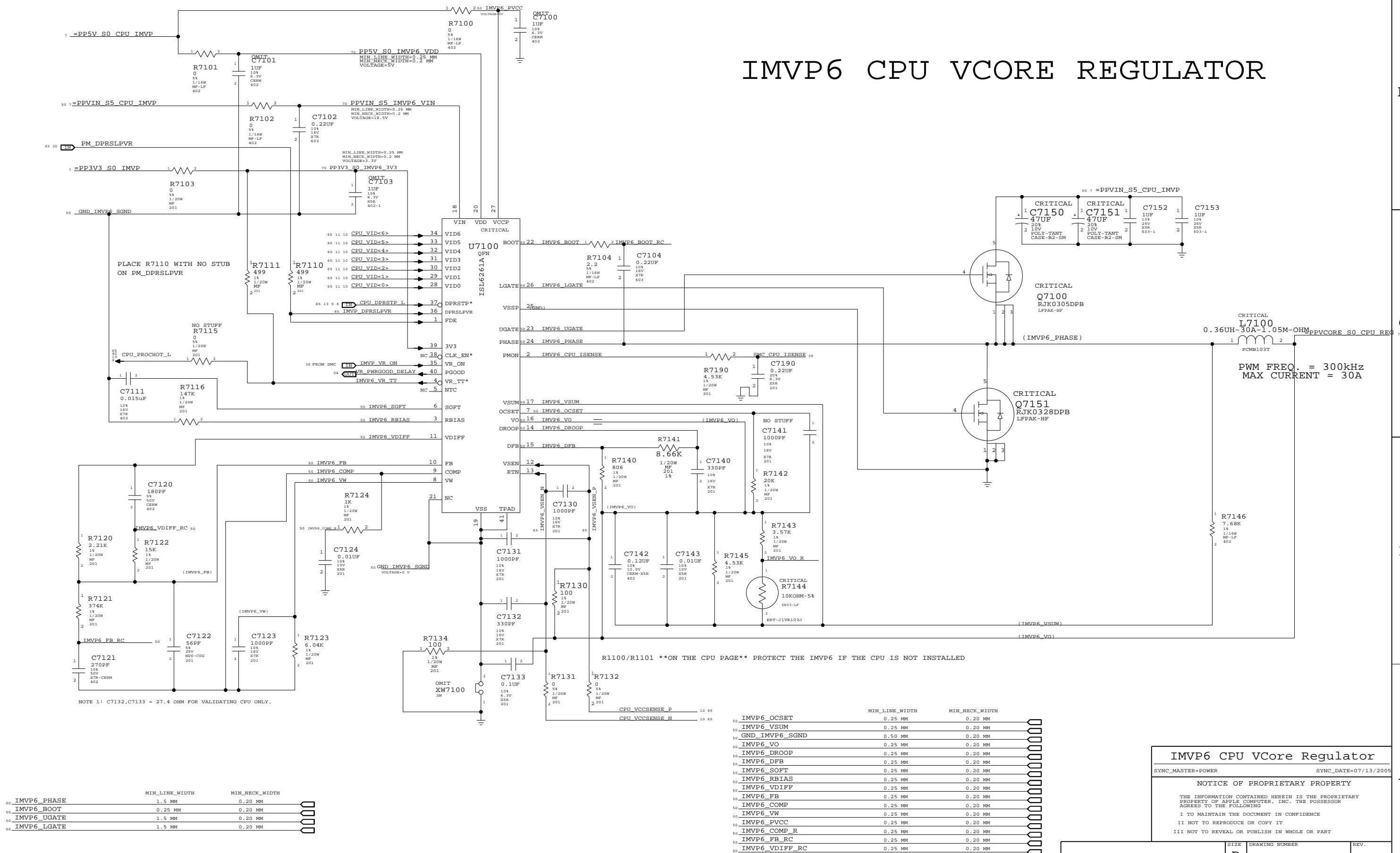
DC-In & Battery Connectors  
SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	49	71

# IMVP6 CPU VCore REGULATOR



## IMVP6 CPU VCore Regulator

SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

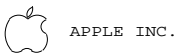
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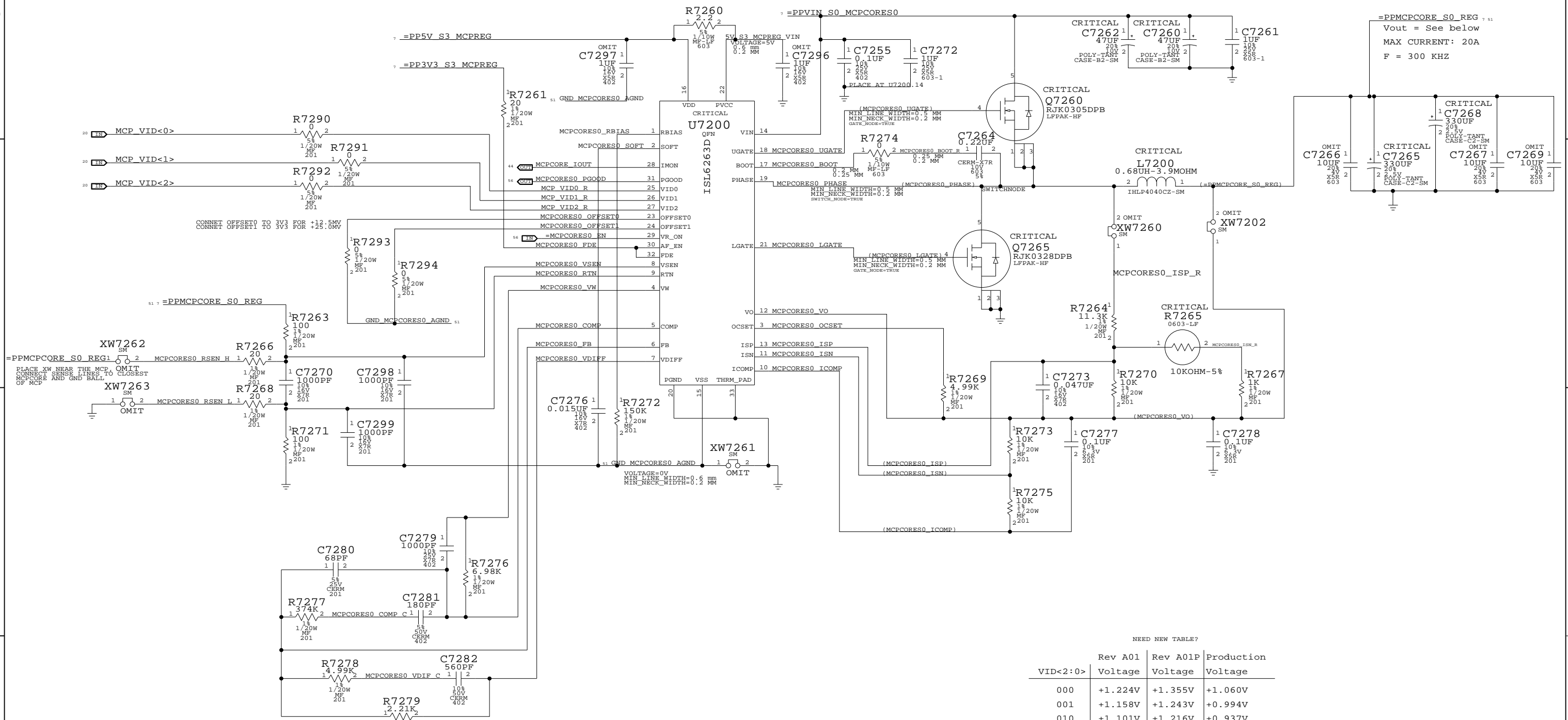
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT 50 OF 71	

# MCP CORE POWER SUPPLY



NEED NEW TABLE?

	Rev A01	Rev A01P	Production
VID<2:0>	Voltage	Voltage	Voltage
000	+1.224V	+1.355V	+1.060V
001	+1.158V	+1.243V	+0.994V
010	+1.101V	+1.216V	+0.937V
011	+1.047V	+1.124V	+0.885V
100	+0.996V	+1.065V	+0.830V
101	+0.952V	+0.994V	+0.789V
110	+0.913V	+0.977V	+0.752V
111	+0.876V	+0.917V	+0.719V

(Also A01Q)

**MCP CORE REGULATOR**

SYNC\_MASTER=MINGJING SYNC\_DATE=06/24/2008

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U7360  
TPS79918  
SON OUT  
CRITICAL  
EN NR  
GND THRM PAD

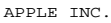
PPVIN\_S0\_P1V8S0  
P1V8S0\_EN  
P1V8S0\_NR  
PP1V8\_S0\_REG  
MAX CURRENT = 200MA

C7360  
1 2  
1uF  
105  
6.3V  
CERM  
402

C7361  
1 2  
0.01uF  
105  
10V  
X5R  
201

C7362  
1 2  
2.2uF  
205  
6.3V  
CERM  
402-LF

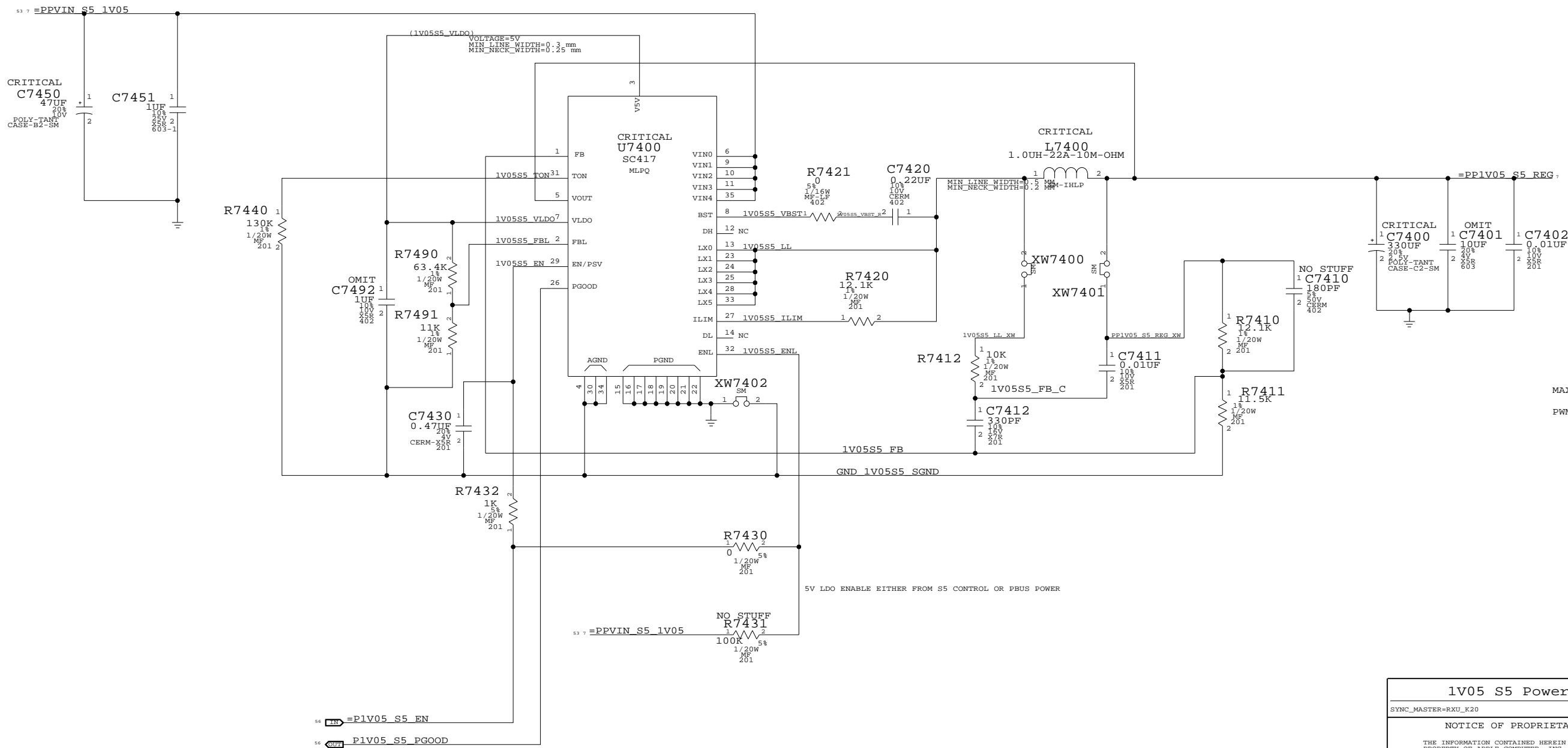
LE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
	SCALE	SHT	OF
	NONE	52	71



SIZE D	DRAWING NUMBER 051-7631	REV. 2.3.0
SCALE NONE	SHT 52	OF 71

# 1V05 S5 POWER SUPPLY

supply for MCP1V05 AUX, FSB (CPU & MCP) VTT, 1V05 S0



MAX CURRENT = 12A  
PWM FREQ = 400KHZ

1V05 S5 Power Supply

SYNC\_MASTER=RXU\_K20

SYNC\_DATE=05/21/2008

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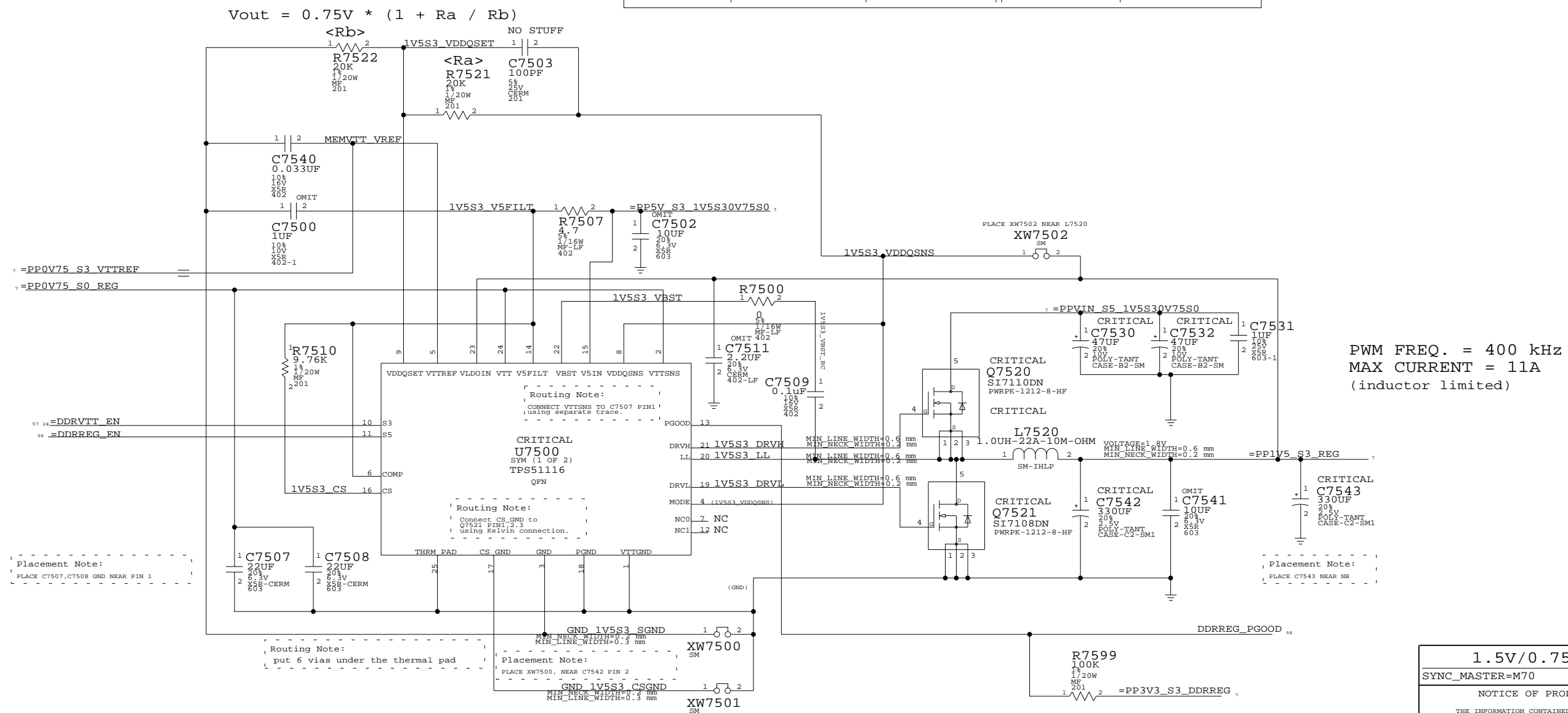
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7631		2.3.0
SCALE		SHT	OF	REV.
NONE		53	71	

# 1.5V/0.75V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



PWM FREQ. = 400 kHz  
MAX CURRENT = 11A  
(inductor limited)

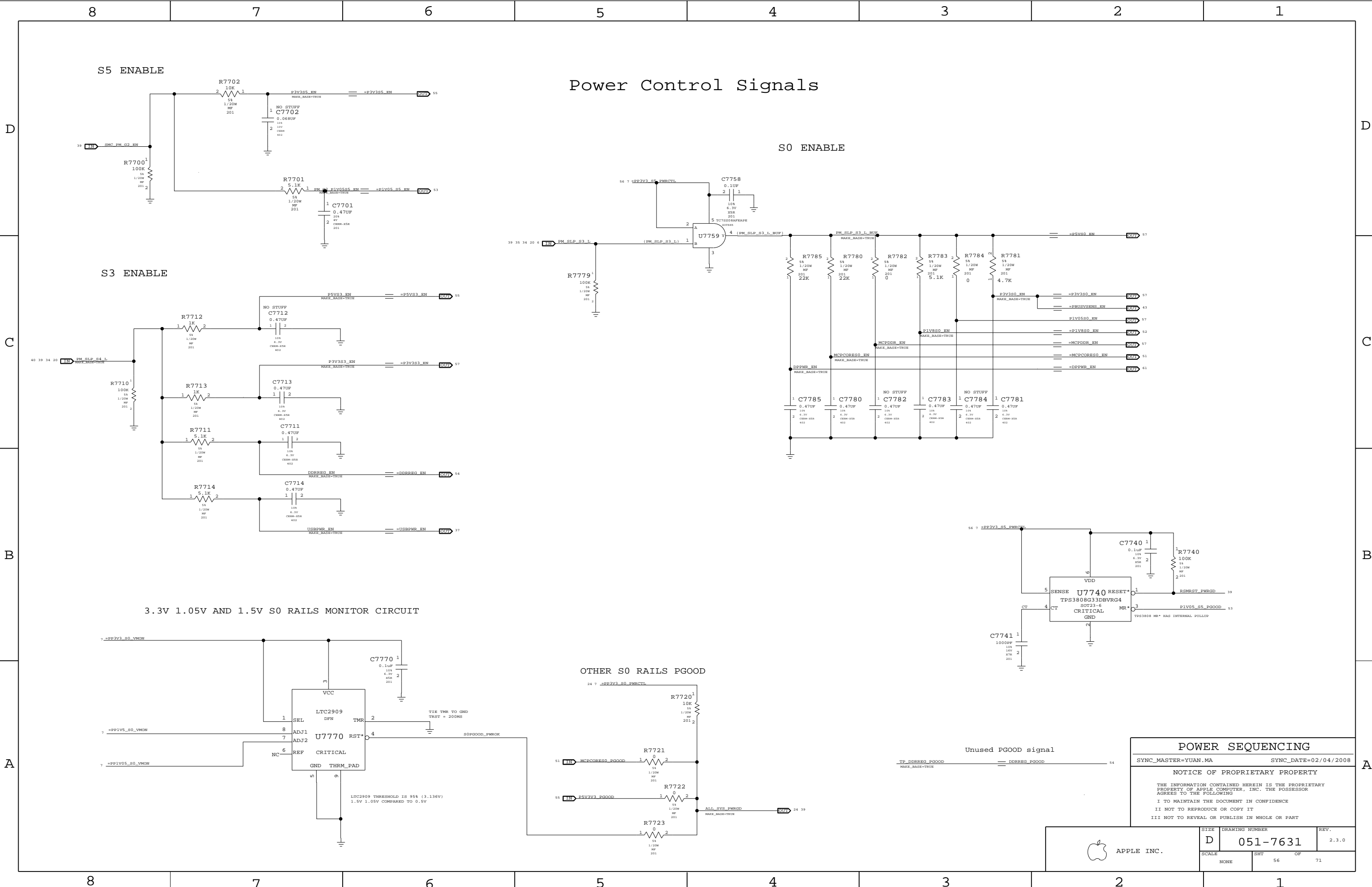
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1.5V/0.75V Supplies
SYNC_MASTER=M70          SYNC_DATE=01/09/2007
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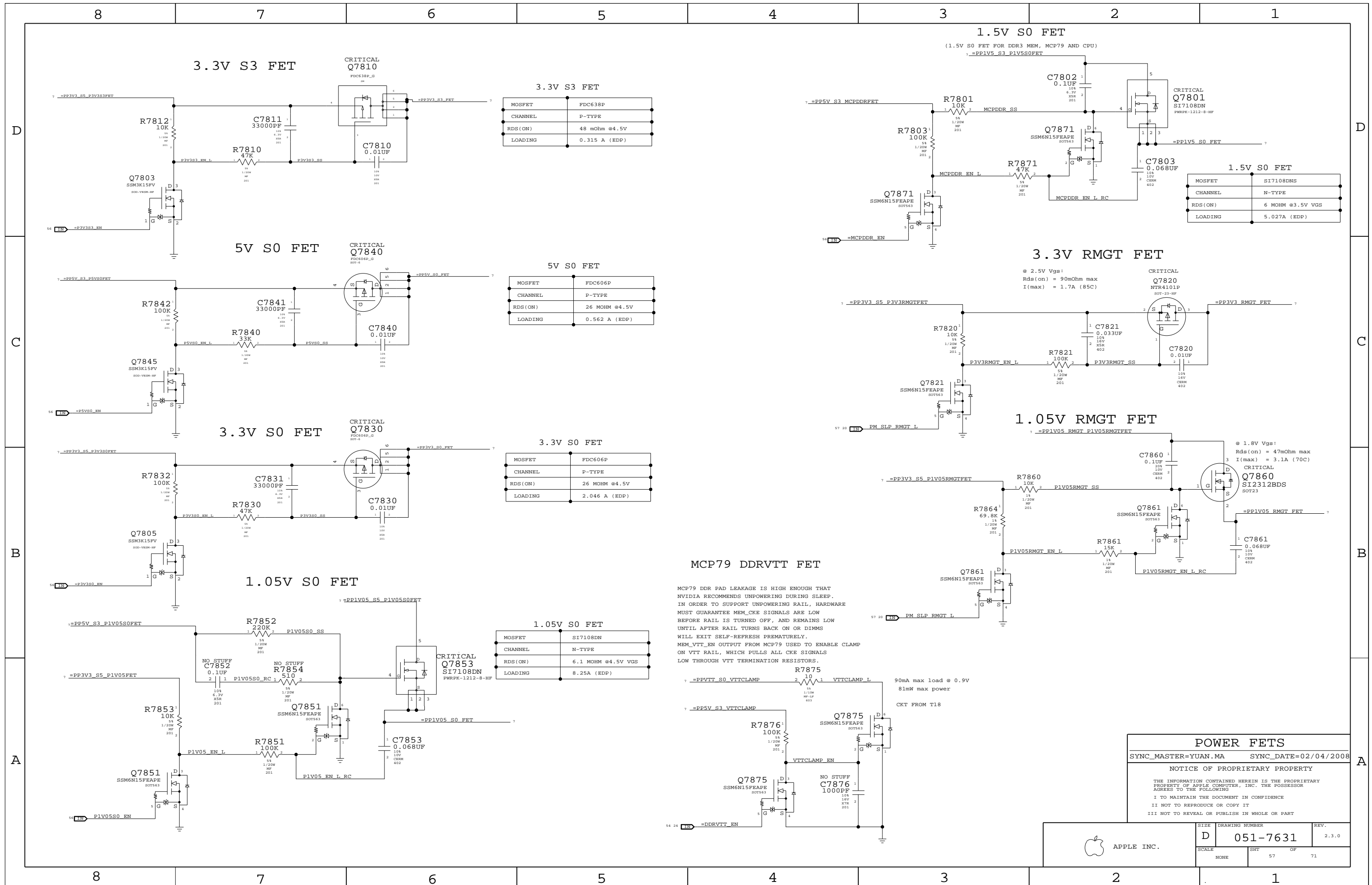
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## D

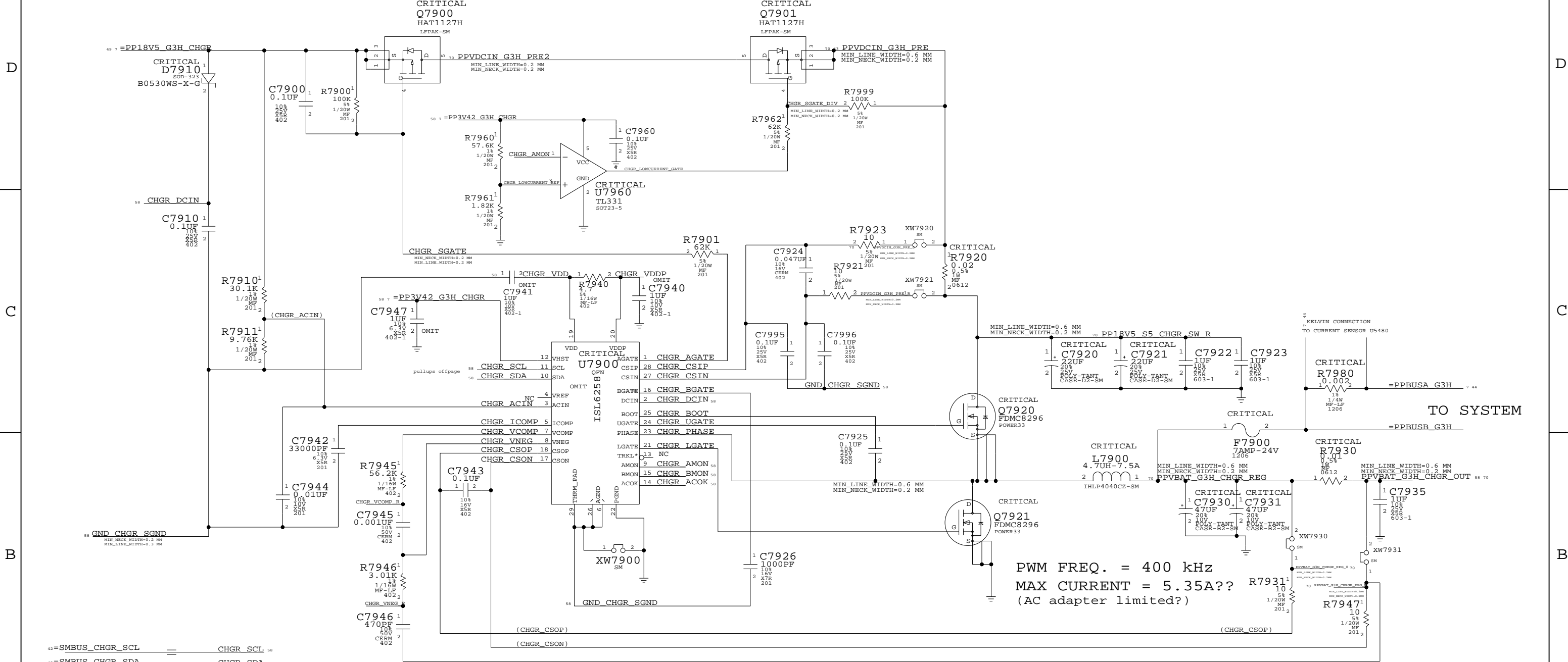
A





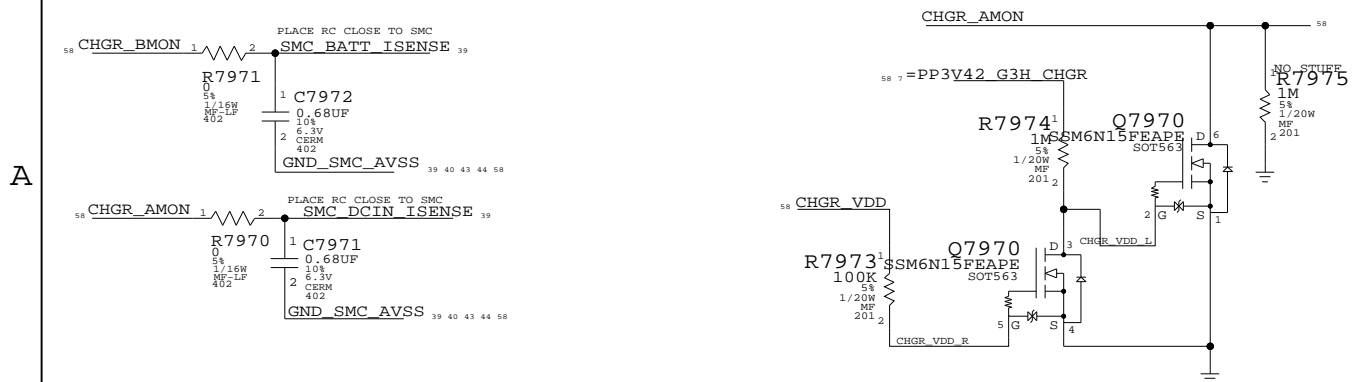


PBUS SUPPLY / BATTERY CHARGER

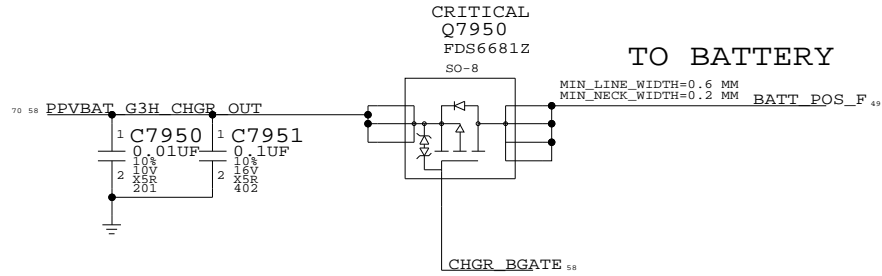


PWM FREQ. = 400 kHz  
MAX CURRENT = 5.35A??  
(AC adapter limited?)

AMON PULLDOWN LOGIC

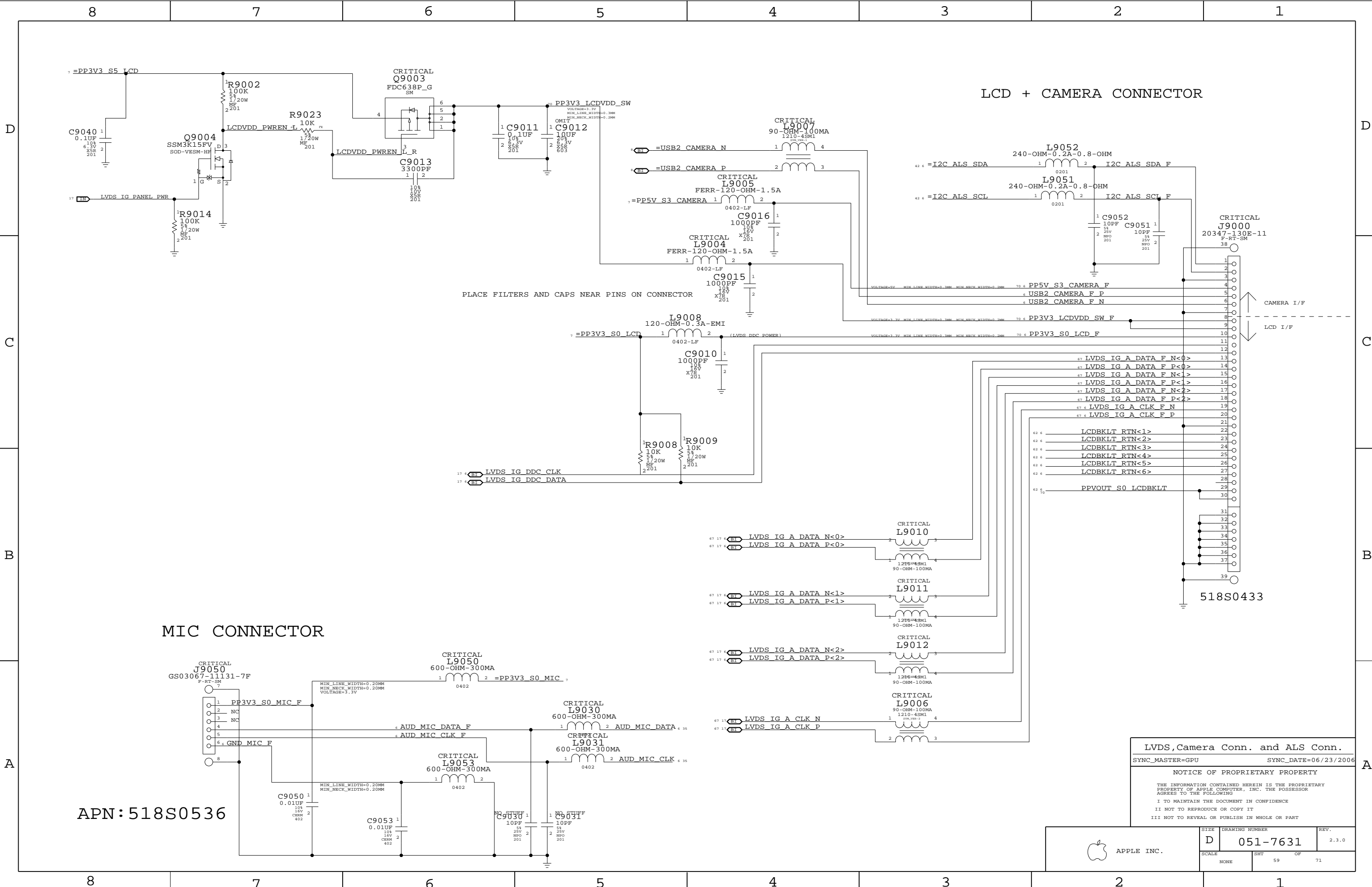


BATTERY CHARGING



PBUS Supply/Battery Charger  
SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
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SCALE		SHT	OF	71
NONE		58		




MIC CONNECTOR

LCD + CAMERA CONNECTOR

APN:518S0536

518S0433

LVDS, Camera Conn. and ALS Conn.  
SYNC\_MASTER=GPU SYNC\_DATE=06/23/2006  
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	SCALE		SHT	OF
	NONE		59	71

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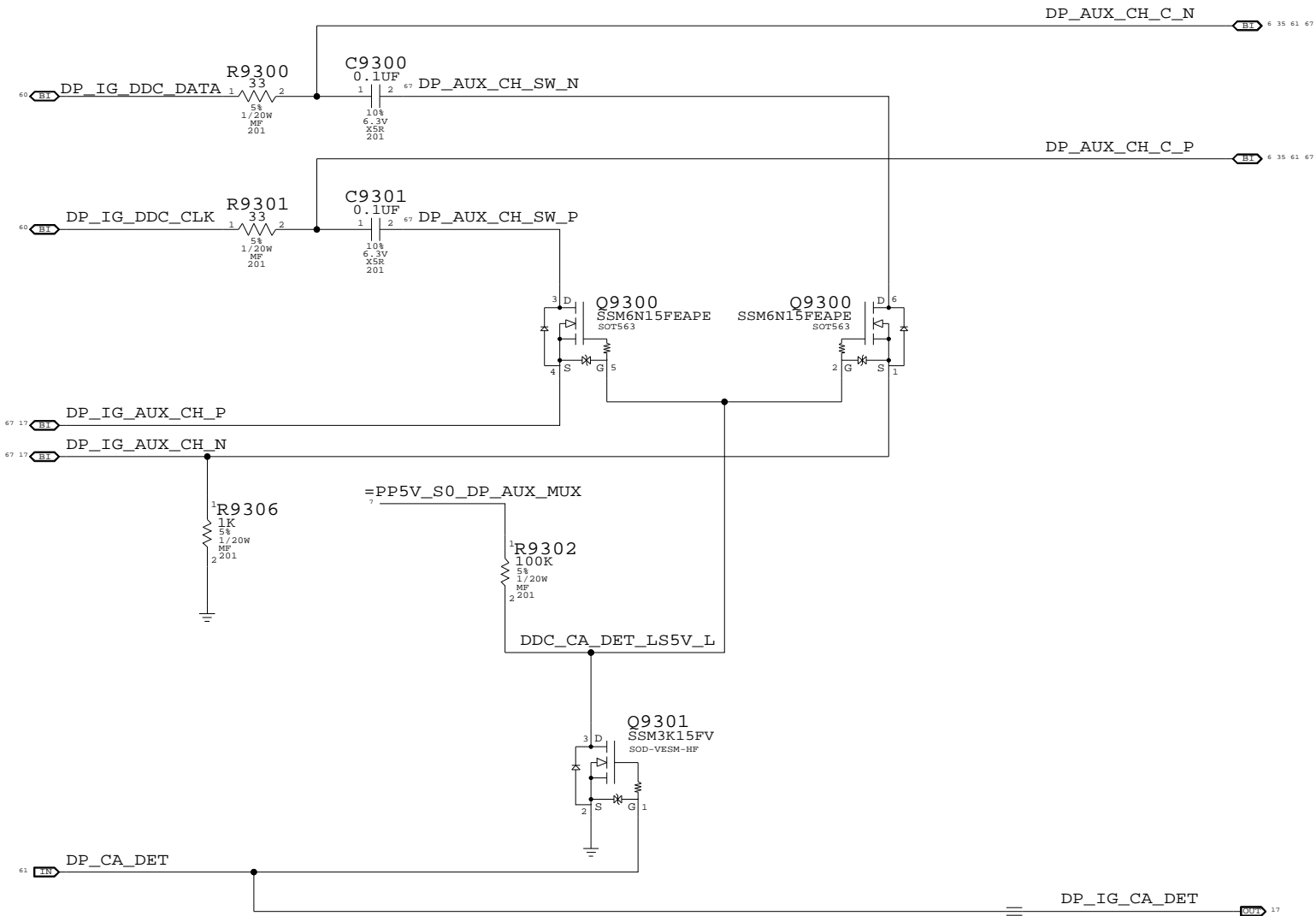
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17	=MCP_HDMI_TXC_P	---	DP_ML_P<3>	---	61	67	
17	=MCP_HDMI_TXC_N	---	DP_ML_N<3>	---	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_P<0>	---	DP_ML_P<2>	---	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_N<0>	---	DP_ML_N<2>	---	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_P<1>	---	DP_ML_P<1>	---	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_N<1>	---	DP_ML_N<1>	---	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_P<2>	---	DP_ML_P<0>	---	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_TXD_N<2>	---	DP_ML_N<0>	---	MAKE_BASE=TRUE	61	67
17	=MCP_HDMI_HPD	---	DP_HPD	---	MAKE_BASE=TRUE	61	
17	=MCP_HDMI_DDC_CLK	---	DP_IG_DDC_CLK	---	MAKE_BASE=TRUE	60	
17	=MCP_HDMI_DDC_DATA	---	DP_IG_DDC_DATA	---	MAKE_BASE=TRUE	60	



DISPLAYPORT SUPPORT

SYNC\_MASTER=NMARTIN SYNC\_DATE=12/18/2007

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SIZE

D

DRAWING NUMBER

051-7631

REV.

2.3.0

SCALE

NONE

SHT

60

OF

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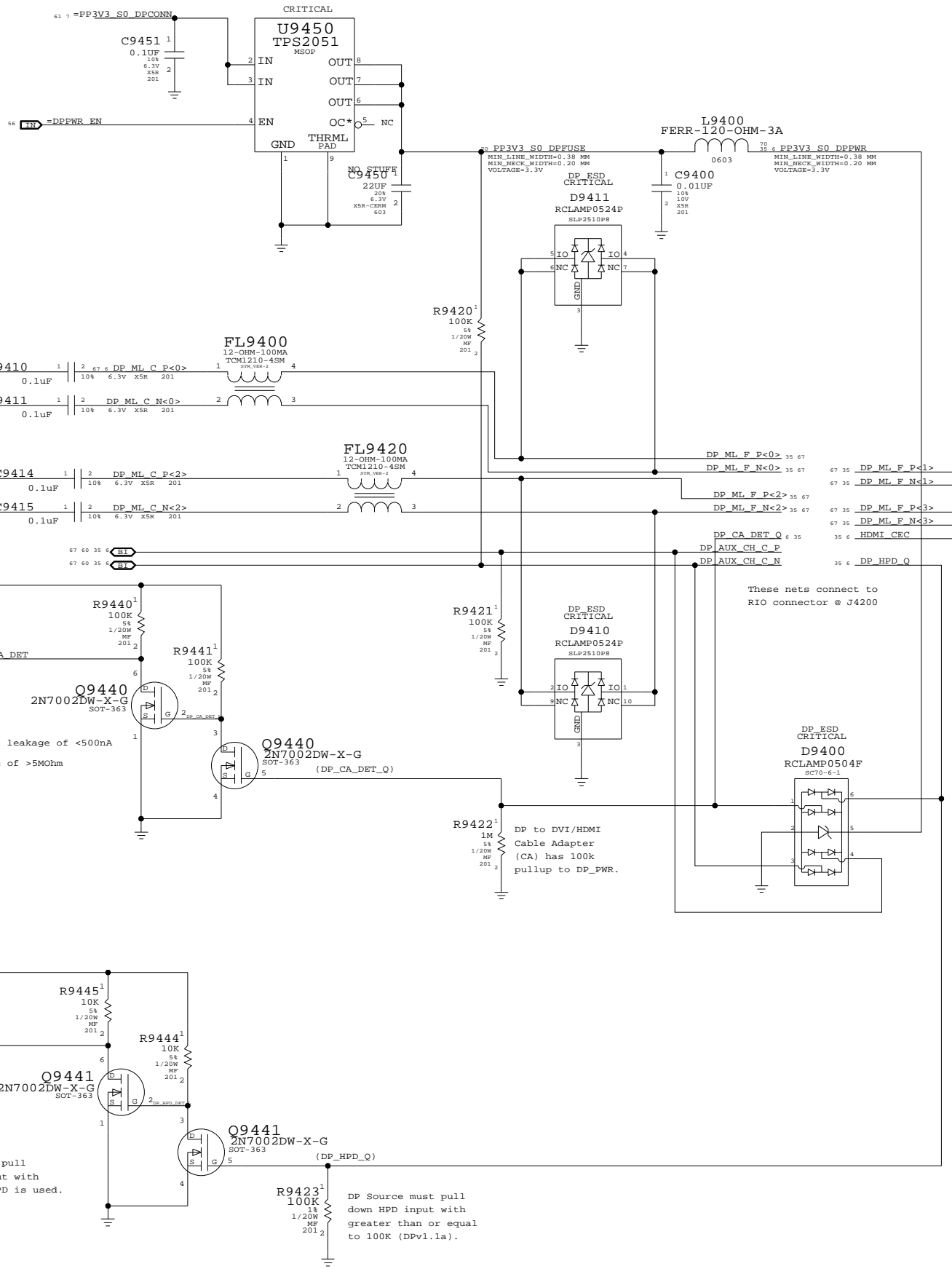
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8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1



DisplayPort Connector

SYNC\_MASTER=M98\_MLB SYNC\_DATE=01/17/2008

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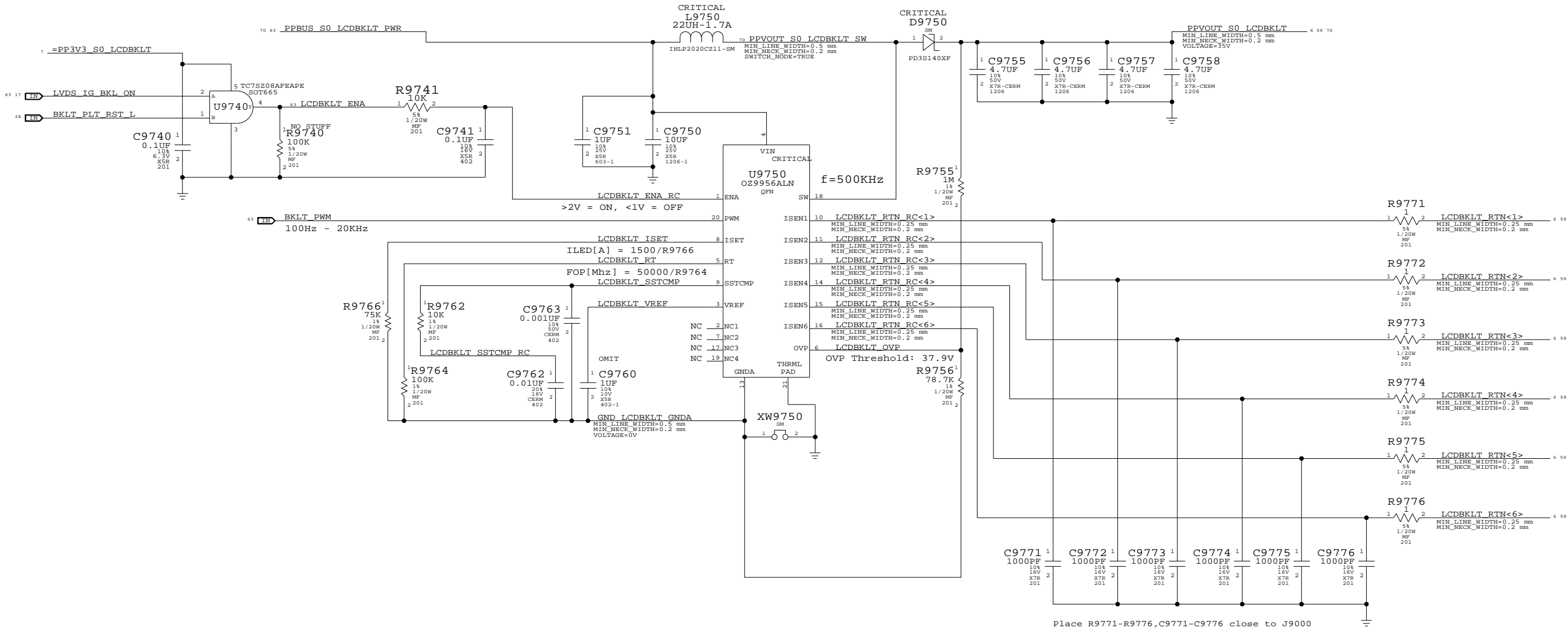
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NONE		61	71

LED Backlight Driver



LED Backlight Driver

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

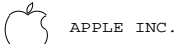
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SCALE	SHT	OF
NONE	62	71







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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.  
Signals within each 4x group should be matched within 5 ps of strobe.  
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.  
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.  
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.  
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.  
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.  
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	9 13
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	9 13
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	9 13
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	9 13
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	9 13
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB BREQ0 L	9 9 13
FSB_BREQ1_L	FSB_50S	FSB_1X	FSB BREQ1 L	13
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	9 13
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	9 9 12 13
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	9 13
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9 9
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	9 13
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9 9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9 9 13
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	9 13 40 50
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	9 12 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	9 13
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM THRMTRIP L	9 13 40
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	9 13
CPU_FERR_SR	CPU_50S	CPU_AGTL	CPU DPSLP L	9 13
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	9 9 13 50
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	9 13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	13
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	9 13
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	9 13
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	6 12 13
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	6 12 13
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	13
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	13
CPU_FERR_L	CPU_50S		CPU IERR L	9
PM_DPRSILPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	20 50
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	50
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	9 25
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	9
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	9
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	6 9 12
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	9 12
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	6 9 12
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	6 9 12
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	6 9 12
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	6 9 12
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	6 9 12
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	6 12
	CPU_50S	CPU_8MIL	CPU VID<6..0>	10 11 50
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>	11
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P	10 50
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N	10 50
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	50
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	50

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FSB 4X Signal Groups

FSB 2X Signals

FSB 1X Signals

CPU/FSB Constraints

SYNC\_MASTER=M97

SYNC\_DATE=02/04/2008

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